Models 545B & 548B
Microwave Frequency Counters

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Warranty

EIP Microwave warrants this product to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level is not covered by the warranty. Removal, defacement, or alteration of any serial or inspection label, marking, or seal may void the warranty. EIP Microwave will repair or replace, at its option, any components of this product which prove to be defective during the warranty period, provided the entire unit is returned PREPAID to EIP or an authorized service facility. In-warranty units will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No warranty other than the above is expressed or implied.

Certification

EIP Microwave certifies this instrument to be in conformance with the specifications noted herein at time of shipment from the factory. EIP Microwave further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology.

Manual Change Information

As EIP continually improves and updates its products, changes to the material covered by the manual will occur. When a part or assembly in an EIP instrument is changed to the extent that it is no longer interchangeable with the earlier part, the Change Control Number (CCN) of the instrument, shown on the title page of the manual, will change and a new edition of the manual will be published. A new edition not involving a CCN change will show the new date on the front page and on each changed page.

Sometimes, due to printing and shipping requirements, changes cannot be incorporated into the printed manual immediately. In these cases, dated change pages will be shipped with the manual. Please insert these pages in your manual and remove the obsolete pages, if any.

Customer Suggestion Form

A mail-in form at the end of this manual provides an easy way for you to tell us about any additions, corrections, or changes that would improve this publication. Your suggestions are a valuable part of the input used in revising our manuals and developing the structure and format for new manuals.

SAFETY

The Model 545B/548B is a Safety Class 1 instrument. This instrument has been designed and tested according to international safety requirements.

This manual contains information, cautions, and warnings that must be followed by the service person to ensure safe operation and to retain the instrument in safe condition.

SAFETY SYMBOLS

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure or practice, which, if not correctly performed or adhered to, could result in personal injury.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure or practice, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

OVERALL SAFETY CONSIDERATIONS

WARNING

Before this instrument is switched on, the protective earth terminals of this instrument MUST be connected to the protective conductor of the ac power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective earth (grounding) conductor.

WARNING

Only fuses with the required rated current voltage and specified type should be used. DO NOT use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.

WARNING

Whenever it is likely that the protection has been impaired, the instrument MUST BE made inoperative and be secured against any unintended operation.

WARNING

All protective earth terminals, extension cords, autotransformers, and devices connected to this instrument should be connected to a socket outlet provided with a protective earth contact. Any interruption of the protection will cause a potential shock hazard that could result in personal injury.

CAUTION

Before connecting power to the instrument, check to insure that the correct fuse is installed and the voltage select switch on the rear panel of the instrument is set properly. Refer to Installation Section 2.

CAUTION

Excessive signals can damage instrument. To prevent damage, do not exceed specified damage level. Refer to specifications listed in Section 1.

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Section 1
General Information

DESCRIPTION

The 545B/548B series counters are microprocesor-based heterodyne instruments. The basic frequency range of the 545B is 10 Hz to 20 GHz, while the 548B extends to 26.5 GHz.

Through keyboard contol, the 54XB series counters provide frequency offsets and frequency selectivity. Options include full systems capability via GPIB, high stability time bases, and frequency extension to 110 GHz for 548B. Measurements are presented on a 12 digit LED display that is sectionalized to read GHz, MHz, kHz, and Hz.

Frequency counting is divided into 3 bands. Band 1 is a high impedance input (1 M ohm/20 pF) and covers 10 Hz to 100 MHz, with a sensitivity of 25 mV RMS. Band 2 has an input impedance of 50 ohms, a 10 MHz to 1 GHz range, and has a sensitivity of -20 dBm. Band 3 has an input impedance of 50 ohm nominal over a range of 1 GHz to 20 GHz on the 545B, and 1 GHz to 26.5 GHz on the 548B.

SPECIFICATIONS

GENERAL	
RESOLUTION	Front panel keyboard input select 0.1 Hz to 1 GHz, 0.1 Hz resolution Band 1 only. No frequency offset or multiplier in 0.1 Hz resolution.
GATE TIME	1 msec for 1 kHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	± 1 count ± time base error
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets (standard) and power offsets (standard with power measurement Option 02). Displayed frequency (power) is offset by entering value to 1 Hz resolution (0.1 dB power).
OPERATION TEMP.	0° C to 50° C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz, 60 VA typical
WEIGHT, NET	~ 26 lb (11.8 kg)
WEIGHT, SHIPPING	~ 32 lb (14.5 kg)
DIMENSIONS (HWD)	3.5" x 16.75" x 14.0" (89 mm x 425 mm x 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

TIME BASE	
FREQUENCY	10 MHz TCXO
AGING RATE	$<\|1 \times 10^{-7}\|$ per month, $<\|1 \times 10^{-8}\|$per year
SHORT TERM	$<1 \times 10^{-9}$ rms for one second averaging time
TEMPERATURE	$<\|1 \times 10^{-8}\|$ 0° to 50° C when set at 25° C
LINE VARIATION	$<\|1 \times 10^{-7}\|$ ± 10% change.
WARM UP TIME	30 minutes
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimum into 300 ohms
PHASE NOISE	-95 dBc/Hz at 10 Hz from carrier

SPECIFICATIONS, continued

BAND 1	
FREQUENCY RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 M ohm/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	1 V rms
DAMAGE LEVEL	150 V rms *
	* (Above 1 kHz damage level will decrease at 6 dB/octave down to 3.0 V rms.)
BAND 2	
FREQUENCY RANGE	10 MHz to 1 GHz
SENSITIVITY	-15 dBm
DYNAMIC RANGE	25 dB
IMPEDANCE	50 ohms Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	<50 msec
BAND 3	
FREQUENCY RANGE	1 GHz to 20 GHz (26.5 GHz for model 548B)
SENSITIVITY	-30 dBm: 1 GHz to 12.4 GHz -25 dBm: 12.4 GHz to 20 GHz -20 dBm: 20 GHz to 26.5 GHz
DYNAMIC RANGE	1 GHz to 12.4 GHz, 40 dB 20 GHz to 26.5 GHz, 30 dB 12.4 GHz to 20 GHz, 35 dB
IMPEDANCE	50 ohms Nominal
CONNECTOR	Model 545B: Precision Type N (female) Model 548B: APC 3.5 (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	10 Watts, (+40 dBm)
ACQUISITION TIME	< 200 msec independent of frequency
AMPLITUDE DISCRIMINATION	10 dB, If <10 dB will count one signal accurately if seperated by >200 MHz.
FM MODULATION	20 MHz p-p up to 10 MHz rate
VSWR	< 2.5: 1 typical

SPECIFICATIONS, continued

OPTIONS

01 DIGITAL TO ANALOG CONVERTER
DAC will convert any three consecutively displayed digits into a 0 to 0.999V output on rear panel.

02 POWER METER
1 TO 20/26.5 GHz will measure power of sine wave to 0.1 dB resolution from sensitivity to −10 dBm; 0.2 dBm resolution from −10 dBm to overload. Power offset to 0.1 dB resolution, selectable from front panel; will not degrade performance of the counter.

NOTE: Power Meter and Source Locking cannot be active at the same time.

TIME BASE OSCILLATORS	03	04	05
AGING RATE/24 HOURS (After 72 hour warm-up)	$<\|5 \times 10^{-9}\|$	$<\|1 \times 10^{-9}\|$	$<\|5 \times 10^{-10}\|$
SHORT TERM STABILITY (1 second average)	$<1 \times 10^{-10}$ rms	$<1 \times 10^{-10}$ rms	$<1 \times 10^{-10}$ rms
0° to +50° C TEMPERATURE STABILITY	$<\|6 \times 10^{-9}\|$	$<\|3 \times 10^{-9}\|$	$<\|3 \times 10^{-9}\|$
±10% LINE VOLTAGE CHANGE	$<\|5 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$

06 EXTENDED FREQUENCY CAPABILITY BAND 4 - 548B ONLY.

FREQUENCY RANGE	26.5 GHz to 110 GHz - See Remote Sensor chart below.
SENSITIVITY (typ)	-25 dBm
CONNECTOR	Depends on Remote Sensor - See Remote Sensor chart below.
MAX. INPUT LEVEL (typ)	+5 dBm
DAMAGE LEVEL	+10 dBm
AMPLITUDE DISCRIMINATION	20 dBm
ACQUISITION TIME (typ)	<1 sec

NOTE: Band 4 requires a Model 590 Cable Kit and one or more remote sensors. See chart below.

08 GPIB — Provides programming and output capability per IEEE 499-1978.

09 REAR INPUT — Signal input connectors on rear panel of counter.

10 CHASSIS SLIDES

BAND 4 REMOTE SENSORS

REMOTE SENSOR	BAND	FREQUENCY RANGE	WAVEGUIDE SIZE	WAVEGUIDE FLANGE
91	41	26.5 - 40 GHz	WR-28	UG-599/U
92	42	40 - 60 GHz	WR-19	UG-383/U
93	43	60 - 90 GHz	WR-12	UG-387/U
94	44	90 - 110 GHz	WR-10	UG-387/U
95	42,43	50 - 75 GHz	WR-15	UG-385/U
96	41,42	33 - 50 GHz	WR-22	UG-383/U

Section 2
Installation

UNPACKING

The EIP 545B/548B series Microwave Frequency Counters arrive ready for operation. Carefully inspect the shipping carton for any sign of visible or concealed damage. If the carton is damaged, immediately notify shipper's agent.

Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the counter, checking for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

INSTALLATION

There are no special installation instructions for these units. The units are self-contained bench or rack mounted instruments, which only require connection to a standard, single-phase power line for operation.

CAUTION

Always be sure that the fuse is the type and value specified, and that the voltage select switch is set to correspond to the AC power input voltage; otherwise, the counter may be damaged.

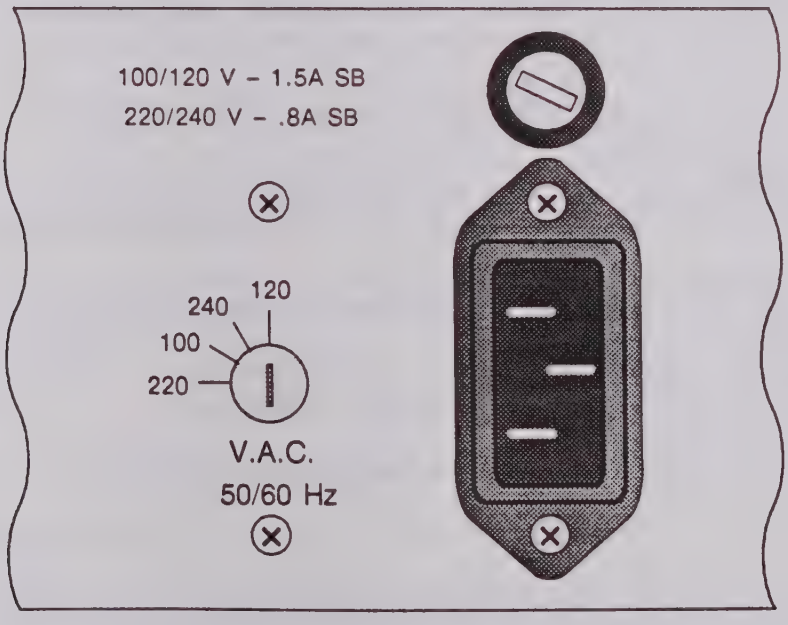


Figure 2-1. Rear Panel Fuse and Voltage Select Locations

VOLTAGE SELECTION

The voltage select switch should be set to the proper line voltage. To change line voltage:

1. Disconnect the counter from the power line.
2. Use a screwdriver to turn the slotted voltage indicator to the desired position.

FUSE REPLACEMENT

The counter uses one fuse. It is located on the rear panel above the line voltage plug. The following fuses must be used:

Line Voltage	Fuse Type
100/120 VAC	1.5A Slow-blow MDL
220/240 VAC	.80A Slow-blow FST

To release the fuse, use a screwdriver to rotate the slotted cap counter-clockwise. To reinstall the fuse, press the fuse and slotted cap assembly into the fuse cavity and turn it clockwise until it locks into place.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure can be performed without special tools or equipment.

1. Turn counter power switch off. Check fuse rating and setting of AC POWER switch on rear panel.

2. Connect power cord to 100/120 or 220/240 V, 50-60 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.

3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that automatic self-check has been completed.

4. Press TEST 0 1 Display should read 200 000 000 ±1.

5. Press TEST 0 2 Display should read all 8's and all annunciators should be lit.

6. Press TEST 0 3 Each display segment should light in turn.

7. Press TEST 0 4 Each digit should light in turn.

8. This completes the performance checkout procedure.

SERVICE INFORMATION

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

CAUTION

Do not attempt repair or disassembly of the Microwave Converter, Millimeter Wave Converter, or Time Base Oscillator assemblies. Such action will void the warranty of the counter. Contact EIP or your sales representative.

COUNTER IDENTIFICATION

This counter is identified by three sets of numbers: the Model Number: 545B or 548B, Serial Number, and a Configuration Control Number. They are located on a label affixed to the frame at the rear of the counter. These numbers must be included in any correspondence regarding your counter

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model, complete serial number, and CCN of the counter.
- A complete description of the problem (Under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptoms?)
- Name and telephone number of someone familiar with the problem that may be contacted by EIP for any further information if necessary.
- Shipping address to which the counter is to be returned. Include any special shipping instructions.

Pack the counter for shipping as detailed below.

SHIPPING INSTRUCTIONS

Wrap the counter in heavy plastic or kraft paper, and repack in original container if available. If the original container cannot be used, use a heavy (275 pound test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of this manual.

Section 3
Operations

INTRODUCTION

The Operations Section of this manual consists of a listing of the controls, connectors, and indicators featured on the Model 54XB Microwave Frequency Counter, followed by an explanation of how each counter function operates, plus some general measurement considerations.

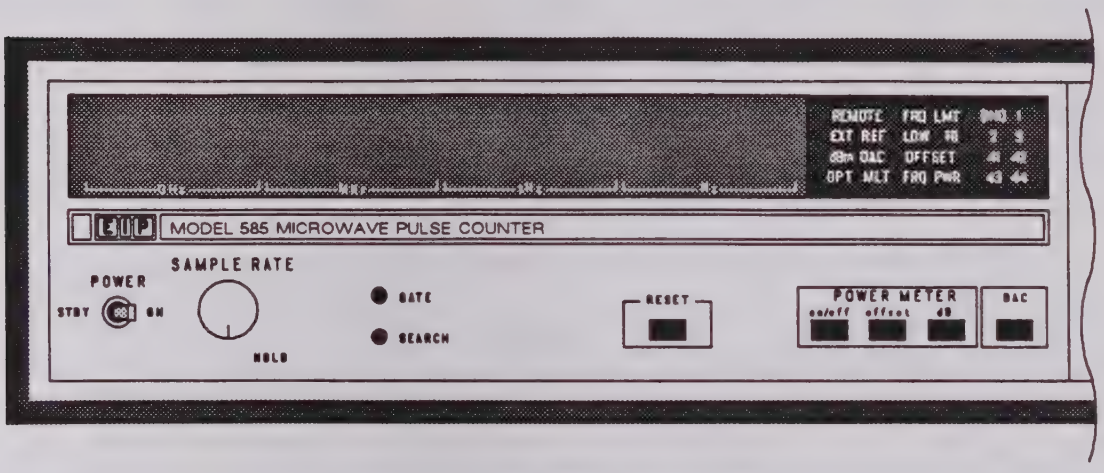


Figure 3-1. Front Panel, Model 548B

FRONT PANEL CONTROLS AND INDICATORS

- POWER switch – turns counter on.
- SAMPLE RATE/HOLD – varies time between measurements from 0.1 to 10 seconds (nominal). (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD until Reset is issued.
- GATE – lights when the signal gate is open and a measurement is being made.
- SEARCH – lights when the counter is not locked to an input signal.
- DATA DISPLAY – The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz. Power information is displayed in dBm to 0.1 dB resolution, on the three right-most digits. When both power and frequency are displayed, frequency resolution is limited to 100 kHz.
- STATUS DISPLAY – a series of annunciators provided to indicate current operating status of the counter.
- KEYBOARD – both data entry and function selection are controlled through the keyboard (see Keyboard Section on page 3-5).

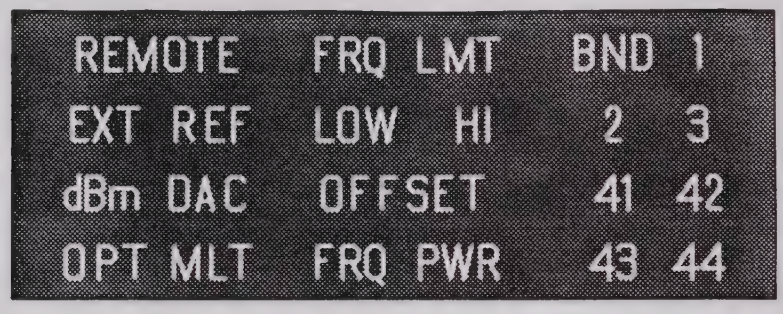


Figure 3-2. Status Display

STATUS DISPLAY

- REMOTE lights to indicate that front panel controls are disabled, and that the counter is being controlled through the GPIB (Option 08).
- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT indicate that correct signal level has been applied.

- dBm lights to indicate that the Power Meter (Option 02) is active.
- DAC lights to indicate that the Digital-to-Analog Converter (Option 01) is active.
- OPT lights to indicate that a special option is active.
- MLT lights to indicate the multiplier function is active.
- FRQ LMT, LOW lights when Band 3 frequency limit low is active.
- FRQ LMT, HI lights when Band 3 frequency limit high is active.
- OFFSET, FRQ lights when frequency offset is active.
- OFFSET, PWR lights when power offset is active.
- BND 1, 2, 3, 41, 42, 43, or 44 lights to indicate which operating range has been selected. When any Band 4 annunciator is lit it indicates that the Extended Frequency Capability, Option 06, has been selected (548B only).

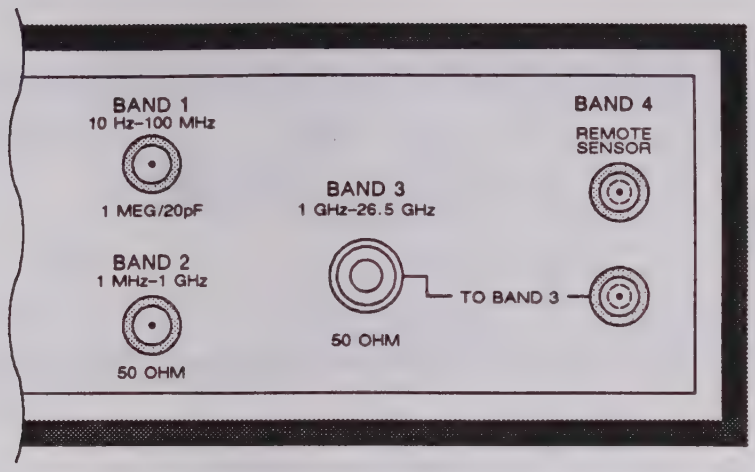


Figure 3-3. Signal Input Connectors, Model 548B

SIGNAL INPUT

- BAND 1 input connector (BNC female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.
- BAND 2 input connector (BNC female) has a nominal input impedance of 50 ohms. It is used for measurements in the range of 10 MHz to 1 GHz.
- BAND 3 input connector on the Model 545B is a precision type N female. It is used for counter operation in the range of 1 GHz to 20 GHz. Model 548B has an APC-3.5 female connector that is used for operation in the range of 1 GHz to 26.5 GHz.
- BAND 4 (Option 06) covers the frequency range of 26.5 GHz to 110 GHz using external remote sensors (see page 1-3) along with two cables contained in the Model 590 Cable Kit. One cable is used to connect the remote sensor to the counter and the other cable is used to connect to Band 4 IF to the Band 3 Input. This option is not available on the 545B.

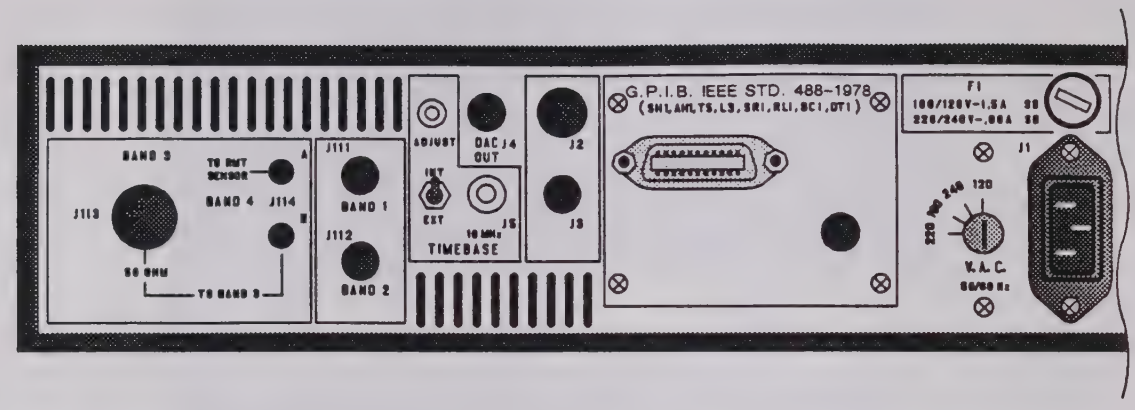


Figure 3-4. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- Spaces labeled BAND 1, BAND 2, BAND 3, BAND 4, and TO RMT SENSOR are used on instruments equipped with Option 09, Rear Panel Input.
- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.
- TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.
- TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.
- DAC OUT connector (BNC female) provides a analog voltage proportional to any specified three digits of frequency displayed, in instruments equipped with Option 01, Digital to Analog Converter.
- GPIB connector is used with the IEEE 488-1978 General Purpose Interface Bus (Option 08).
- F1 fuse providing overload protection.
- VAC SWITCH sets the operating voltage of the counter to match power line.

CAUTION

Switch setting and fuse rating must match power line voltage. Refer to Installation Section for more information.

- AC POWER connector accepts the power cord supplied with the counter.

INSTRUMENT DEFAULT SETTINGS

When the counter is initially turned on the state of the counter is determined by a set of default values which are stored in memory. The factory-set values are listed below.

Parameter	Default Value
Band	3 (Microwave Band)
Sub-Band	1
Resolution	0 (1 Hz)
Frequency Multiplier	01
Frequency Offset	0 Hz
Frequency Limit Low	950 MHz
Frequency Limit High	20.5 GHz (Model 545B) 26.7 GHz (Model 548B)
Frequency Display	On

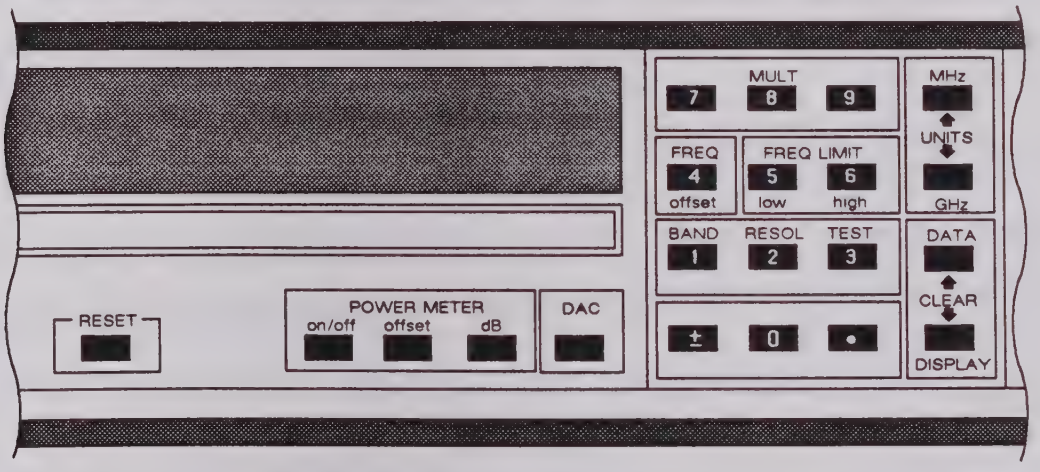


Figure 3-5. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry—the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset, frequency limits, or phase lock frequency. The CLEAR DATA and CLEAR DISPLAY keys are also used to clear stored or displayed data. Twelve of the keys are also used to select the band, resolution, test function, frequency offset, frequency limits, multiplier, band width, lock frequency, phase lock, store, and recall function.

RESET

RESET is a dual function key. When the counter is in remote, pressing the RESET key once causes the counter to return to local. When in local, pressing the RESET key resets the counter and converter, and initiates a new measurement.

POWER METER

Three keys control the optional power measurement function.

PRESS: [on/off] — Activates/deactivates power meter.

PRESS: [offset] — Activates the power offset function.

PRESS: [dB] — Acts as a terminator for the input of power offsets.

DAC

To enable the optional DAC, Digital to Analog Converter, press the DAC key followed by two digits (01–12). The number keyed in will select the most significant digit.

PRESS: [DAC] [0] [3] — Causes the 1 kHz, 100 Hz, and 1 Hz digits to be selected.

PRESS: [DAC] [0] [9] — Causes the 1 MHz, 100 kHz, and 10 kHz digits to be selected.

PRESS: [DAC] [0] [0] — Turns the DAC off.

UNITS (MHz/GHz)

The MHz and GHz keys act as terminators for the input of frequency offset, frequency limits, or phase lock frequency.

PRESS: [MHz] — Completes Entry Sequence

PRESS: [GHz] — Completes Entry Sequence

CLEAR (DATA/DISPLAY)

PRESS: [DATA CLEAR] — Return "STORED" data of selected function to Power On state. Clears Limits (Low/High), Offsets, DAC, multiplier, band width, lock frequency, and stored phase lock information.

PRESS: [CLEAR DISPLAY] — Clears display. Does not affect stored data. Restores counter to display measurement. Clears entry if counter is in data entry mode.

COUNTER CONTROL FUNCTIONS

BAND SELECTION

The "BAND" KEY followed by a numeric key enables the following band selection on model 545B or 548B.

PRESS: BAND [1] — 10 Hz – 100 MHz Input

PRESS: BAND [2] — 10 MHz – 1 GHz Input

PRESS: BAND [3] — 1 GHz – 20 GHz (Model 545B) 26.5 GHz (Model 548B)

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

On the model 548B equipped with Option 06, a 590 cable kit and appropriate optional remote sensor, Band 4 is selected by:

PRESS: BAND [4] [X]

X should be a number between 1 and 4.

RESOLUTION/GATE TIME SELECTION

The "RESOL" key followed by a numeric key enables following resolutions.

PRESS: RESOL [0] — 1 Hz RESOLUTION

PRESS: RESOL [1] — 10 Hz RESOLUTION

PRESS: RESOL [2] — 100 Hz RESOLUTION

PRESS: RESOL [3] — 1 KHz RESOLUTION

PRESS: RESOL [4] — 10 KHz RESOLUTION

PRESS: RESOL [5] — 100 KHz RESOLUTION

PRESS: RESOL [6] — 1 MHz RESOLUTION

PRESS: RESOL [7] — 10 MHz RESOLUTION

PRESS: RESOL [8] 100 MHz RESOLUTION

PRESS: RESOL [9] 1 GHz RESOLUTION

0.1 HZ RESOLUTION

In order to extend the resolution to 0.1 Hz in Band 1, the gate time, of the counter, is increased to 10 seconds. Therefore, if the count chain reads 11 after the 10-second gate period, then the frequency displayed is 1.1 Hz.

The significance of the digits on the front panel is shifted left three digits. If the frequency of the input signal is 9 MHz, the counter displays 9 GHz.

If the user changes the resolution during the 10-second gate period, the counter still has to wait for the 10-second gate to complete before it changes the gate time accordingly.

To change the counter gate time to 10-seconds through front panel:

PRESS: BAND [1] Selects Band 1.

PRESS: RESOL [.] [1] 0.1 Hz RESOLUTION

To change the counter gate time to 10-seconds via GPIB:

Command the counter "B1R.1".

FREQUENCY LIMITS

Enables entry of frequency limits to 10 MHz resolution. The converter is reset after the entry sequence.

TO INPUT FREQUENCY LIMITS

PRESS: FREQ LIMIT low — Notice flashing annunciator and frequency low limit last entered.

PRESS: [#] — Number keys corresponding to desired frequency low limit to 10 MHz resolution.

PRESS: MHz or GHz — To terminate input sequence. (Notice FRQ LMT LOW annunciators solidly lit after terminator key is released.)

PRESS: FREQ LIMIT high — Notice flashing annunciator and frequency limit high last entered.

PRESS: [#] — Number keys corresponding to desired frequency high limits to 10 MHz resolution.

PRESS: MHz or GHz — To terminate input sequence. (Notice FRQ LMT HI annunciator solidly lit after terminator key is released.)

TO RECALL STORED LIMITS

PRESS: FREQ LIMIT low or FREQ LIMIT high — Stored frequency limit low/high is displayed on front panel.

PRESS: CLEAR DISPLAY — Returns counter to display measurements.

TO REMOVE FREQUENCY LIMITS

PRESS: FREQ LIMIT low, CLEAR DATA or FREQ LIMIT high, CLEAR DATA

NOTE

High and low limits should be separated by at least 100 MHz.

DATA MANIPULATION FUNCTIONS

FREQUENCY OFFSET

Frequency offset function enables the entry of a positive or negative frequency offset to 1 Hz resolution. The offset will be incorporated into the frequency measurement after the next gate.

TO INPUT FREQUENCY OFFSETS

PRESS: FREQ OFFSET — Notice flashing annunciator and frequency offset last entered.

PRESS: # — Number keys corresponding to desired offset frequency to 1 Hz resolution.

PRESS: MHz or GHz — To terminate input sequence. Notice OFFSET FRQ annunciator solidly lit after terminator key is released.

TO RECALL STORED OFFSET

PRESS: FREQ OFFSET — Stored offset is displayed.

PRESS: CLEAR DISPLAY — Returns counter to display measurements.

TO REMOVE FREQUENCY OFFSETS

PRESS: FREQ OFFSET, CLEAR DATA or FREQ OFFSET, 0, GHz or FREQ OFFSET, GHz

MULTIPLY FUNCTION

The multiply function multiples the measured frequency by a positive integer up to 99. The result is displayed to 1 KHz resolution. The multiplier will be incorporated into the frequency measurement after the next gate.

TO ENTER A MULTIPLIER

PRESS: FREQ / MULT — Notice flashing annunciator and multiplier last entered.

PRESS: # # — Number keys corresponding to desired multiplier. Notice MLT annunciator solidly lit after second key is released.

EXAMPLE FREQ / MULT 0 2 FOR MULTIPLIER = 2

TO CLEAR THE MULTIPLIER FUNCTION

PRESS FREQ / MULT CLEAR / DATA or PRESS FREQ / MULT 0 1

TO RECALL MULTIPLIER

PRESS: FREQ / MULT — Stored frequency multiplier is displayed on front panel.

PRESS: CLEAR / DISPLAY — Returns counter to display measurements.

mX±B

By using the frequency offset and multiply functions the counter can automatically perform mX ±B calculations.

The equation for the function performed is:

Displayed Reading = mX±B where m = Multiplier (0 to 99) entered from keyboard.
X = Input frequency.
±B = Frequency offset entered from the keyboard.

To do mX±B calculation for m = 2, b = 70 MHz

PRESS: FREQ / MULT 0 2 and FREQ / OFFSET 7 0 MHz

TEST SELECTIONS

This counter incorporates an automatic power-on self-test along with a variety of performance, calibration and troubleshooting tests accessible from the front panel.

POWER ON TESTS

The power on tests verify proper operations of most functional areas of the counter. As part of the power on tests, the counter checks its RAM and PROM memory. During these tests, dashes are displayed on the front panel. If the RAM test fails, the counter will display all "Es" which indicates that either the RAM or RAM decoding circuit is faulty. If the PROM test fails, the error message will be displayed indicating that either the PROM or the PROM decoding circuitry is faulty. If all tests pass, the counter will begin normal operation about one second after turn-on.

TEST FUNCTIONS

In addition to the power on tests the counter features a variety of other performance, calibration, and configuration tests accessible via the test key on the front panel. The following is a list of these tests:

TEST 01 --- 200 MHz Self Test

This function is used to verify that the Count Chain, Gate Generator, and the VCO are operational.

To activate this test:

PRESS: TEST 0 1

When this function is entered, the counter will do the following:

1. Exit the current band.
2. Set the hardware to the self-test mode.
3. Set the VCO to 400 MHz.
4. Set the counter to take frequency measurements only.
5. Start measurement cycles.

The display will show the frequency measurement results. These results will be output to the GPIB interface when frequency readings are requested. The measurement result should be 200 MHz ±1 count.

TEST 02 --- Light Display Segments

This test will light all LEDs, annunciators and decimal points. It is used to verify that everything on the display will light, to check the intensity of the display and to align the LEDs and annunciators.

To activate this test:

PRESS: TEST 0 2

TEST 03 --- Scan Display Segments

This test lights one segment of each digit and one annunciator in each bank at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate control. It is used to verify that each segment of the display, segment drivers, and display multiplexer operates properly and independently.

To activate this test:

PRESS: TEST 0 3

TEST 04 --- Scan Display Digits

This test lights one entire digit, and its decimal point at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate control. It is used to check each digit and digit driver independently, and verifies operation of the display multiplexer.

To activate this test:

PRESS: TEST 0 4

TEST 05 --- Keyboard Test

This function is used to verify the operation of the keyboard.

After this function is activated, the counter will stop normal operations. The display will show the key code of the last key pressed. When a new key is pressed, the display will be updated to show the code of the new key. When the GPIB controller requests a key code, the code of the last key pressed will be output. (If the controller requests a key code, the counter will output to the GPIB interface the code of the last key pressed even if Special Function 05 is not activated). If the counter is in LOCAL, this function must be terminated by the CLEAR DISPLAY key. If it is in remote, this function can be terminated by any device-dependent command.

To activate this test:

PRESS: TEST 0 5

TEST 06 --- Converter Ramp Test

This test continuously ramps the Band 3 Converter DAC through its range. It is used to test the YIG DAC, YIG drivers, YIG, and Band 3 RF level circuits.

To activate this test:

PRESS: TEST 0 6

TEST 07 --- Sweep VCO test

This test cycles the VCO from 400 to 500 MHz in increments of 50 kHz. The cycle rate can be adjusted using the sample rate control. It is used to test the VCO and phase lock circuitry.

To activate this test:

PRESS: TEST 0 7

TEST 08 --- Power Meter Offset Test

This test is used to set the power meter zero DAC to any setting. The setting is entered as a four digit hexodecimal number. The first two digits are use to program the coarse offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in troubleshooting power meter circuitry.

To activate this test:

PRESS: TEST 0 8

TEST 09 --- Power Meter Gain Test

This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexadecimal number in the following format.

1st digit	A107U10 bits 4-7
2nd digit	A107U10 bits 0-3
3rd digit	A107U12 bits 4-7 (Power Meter Option only)
4th digit	A107U12 bits 0-3 (Power Meter Option only)
5th digit bit 0	Sets Amp marked "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marked "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0-3. Test 09 is used to test the RF level and power meter circuits.

To activate this test:

PRESS: TEST 0 9

TEST 10 --- Memory Read/Alter Routine

Thest 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexadecimal number. When the 4th digit is entered the counter will display the contents of the desired address. The contents are than changed by entering a two digit hexadecimal number.

NOTE

Access to this test is controlled by an internal memory protect switch. Attempting to access this test without switching the memory protect switch will cause the counter to generate an error message.

TEST 90 --- Display and/or Alter GPIB Address

When this function is activated, the counter displays the current address of the GPIB interface. If the address does not need to be changed, the function may be terminated by pressing the CLEAR DISPLAY or CLEAR DATA keys.

After this function has been activated, the GPIB address can be changed by entering a two-digit number between 01 and 99 inclusively.

To activate this test:

PRESS: TEST [9] [0]

Next enter the two digit number corresponding to the desired GPIB address and press CLEAR DISPLAY to exit the test.

TEST 91 --- YIG DAC Automatic Calibration

This function is used to calibrate the Band 3 input filter. Refer to the Service Section for complete information.

NOTE

Access to this test is controlled by an internal memory protect switch. Attempting to access this test without switching the memory protect switch will cause the counter to generate an error message.

TO EXIT TESTS

PRESS: CLEAR DISPLAY — To exit a test and return to normal operation

MUTUALLY EXCLUSIVE FUNCTIONS

There exists in the counter some functions that are mutually exclusive, i.e., when one is active, the others cannot be active at the same time. The following is a list of such functions.

1. When self test is active, all other functions are inactive. The exception is in TEST 01—the RESOLUTION function continues to stay active. If any key is pushed when the counter is in self test, the TEST function will automatically be terminated.

2. The POWER METER function will be terminated whenever BAND 1, 2, or 4 is selected.

SIGNAL MEASUREMENTS WITH THE 545B/548B

AUTOMATIC FREQUENCY MEASUREMENTS

To measure the frequency of a CW signal, apply the signal to input connector that corresponds to the frequency being measured and select the appropriate band. The counter will then proceed to automatically find the signal, measure it and display the measured frequency.

MULTIPLE SIGNAL MEASUREMENTS

In actual microwave environments there are often multiple signals present. In a multi-signal environment the counter will automatically find and measure the largest signal, as specified by amplitude discrimination.

On Band 3, the counter can also measure signals other than the largest signal present. This is accomplished by setting frequency limits around the desired signal. Figure 3-6 shows an example of the frequency limits feature.

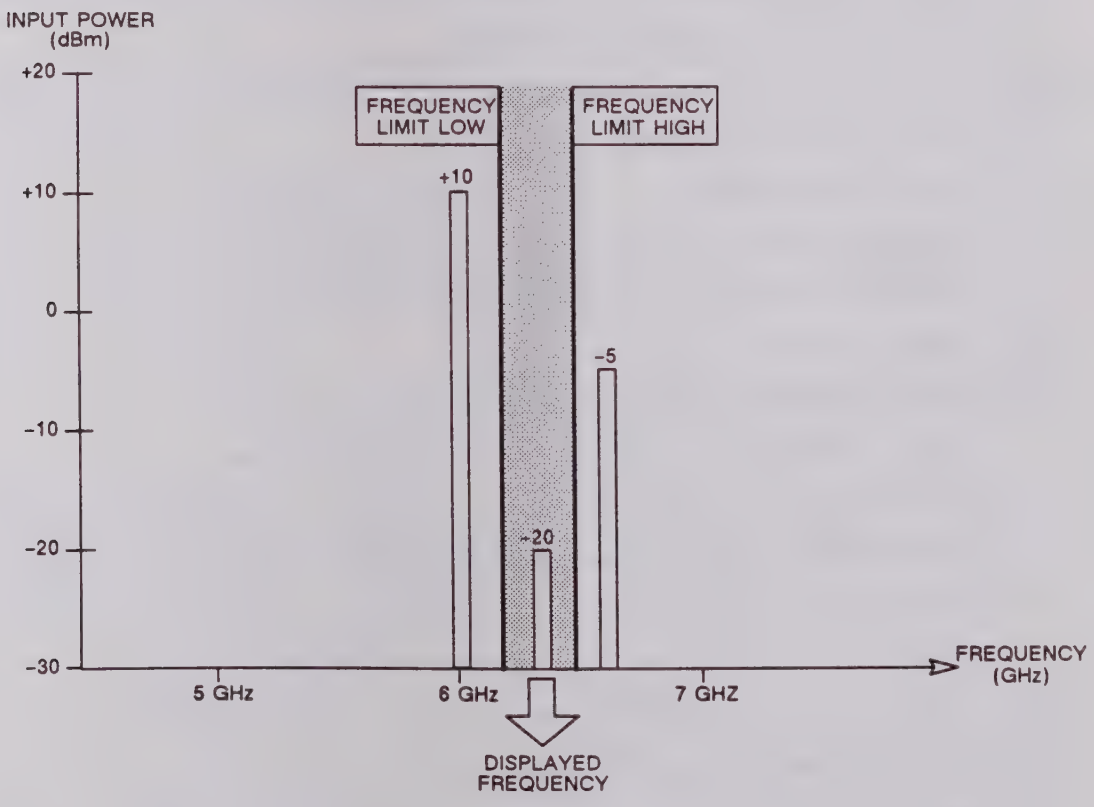


Figure 3-6. Frequency Limits

If the signals shown in Figure 3-6 are applied to Band 3 of the counter, it will automatically find the signal at 6 GHz since it is the largest signal. If it is desired to measure the signal at 6.3 GHz, set the low frequency limit at 6.2 GHz and the high frequency limit to 6.4 GHz. This will prevent the counter from seeing either the signal at 6 GHz or the signal at 6.6 GHz.

ERROR MESSAGES

When an error occurs, the error number will be displayed. The probable cause of each error is listed below.

OPERATOR ERRORS

The following error messages indicate an operator error.

01 Illegal Key Sequence.

02 A resolution number was not entered.

03 A band number was not entered; or the number entered was too large.

04 No power reading in current band.

05 Frequency limit high > 20.5 GHz, 27 GHz (548B).

06 (Freq Limit HI) – (Freq Limit Lo) <100 MHz.

07 Frequency Limit Low <.95 GHz (545B/548B).

08

09 Illegal test mode key sequence.

10 Illegal DAC key sequence.

11 Illegal Multiplier key sequence.

12 SERVICE REQUEST condition input error (GPIB only).

13 Option not installed.

14 Phase lock frequency out of range of current band.

15 Cannot store phase lock information. Counter not phase locked.

16 Storage register 0 does not exist.

17 Illegal BANDWIDTH key sequence.

19 function not allowed in 0.1 resolution.

20 access to this function protected by memory protect switch.

40 DAC table error, cannot find YIG frequency.

41 calibration frequency error.

42 signal not found.

COUNTER ERRORS

The following error messages indicate a malfunction within the counter.

30 EEPROM error.

31	Check sum error	Section 1 PROM	C000–CFFF	A105, U14
32	Check sum error	Section 2 PROM	D000–DFFF	A105, U13
33	Check sum error	Section 3 PROM	E000–EFFF	A105, U17

Section 4
Theory of Operation

GENERAL

The 545B and 548B counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 20 GHz for the 545B, and 10 Hz to 26.5 GHz for the 548B. The frequency range is divided into three bands in both models.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a heterodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 20 GHz (or 26.5 GHz) and uses a YIG tuned heterodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 127 MHz.

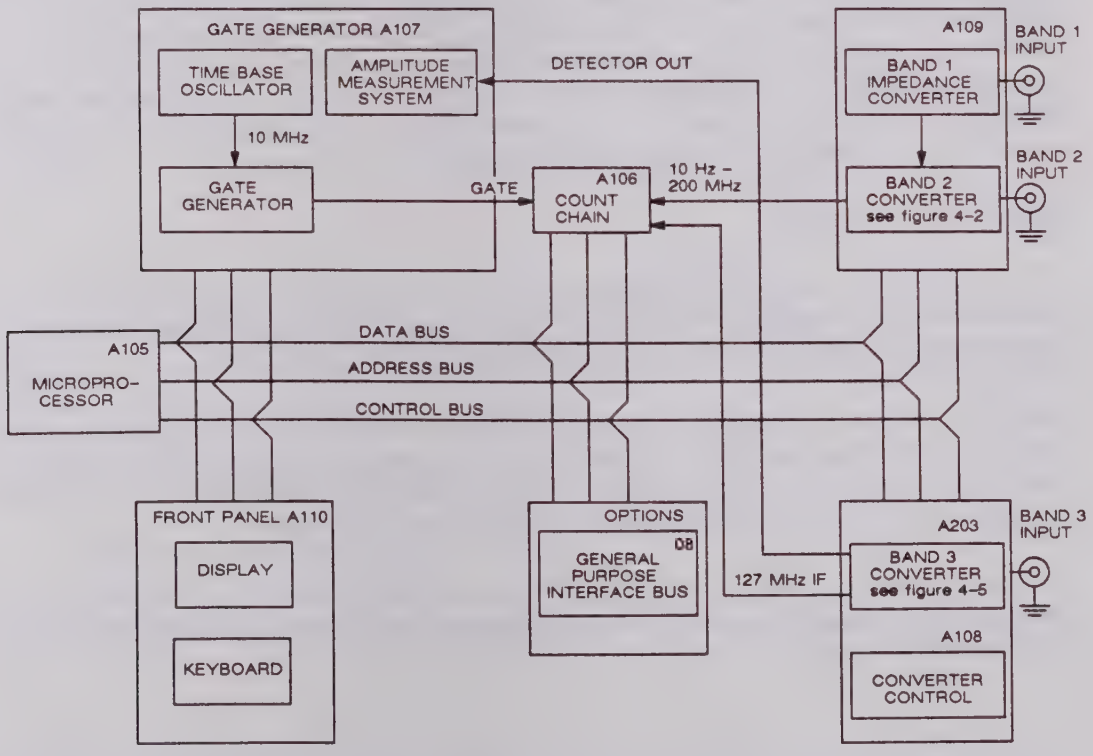


Figure 4-1. Counter Block Diagram, Simplified

BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information, band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

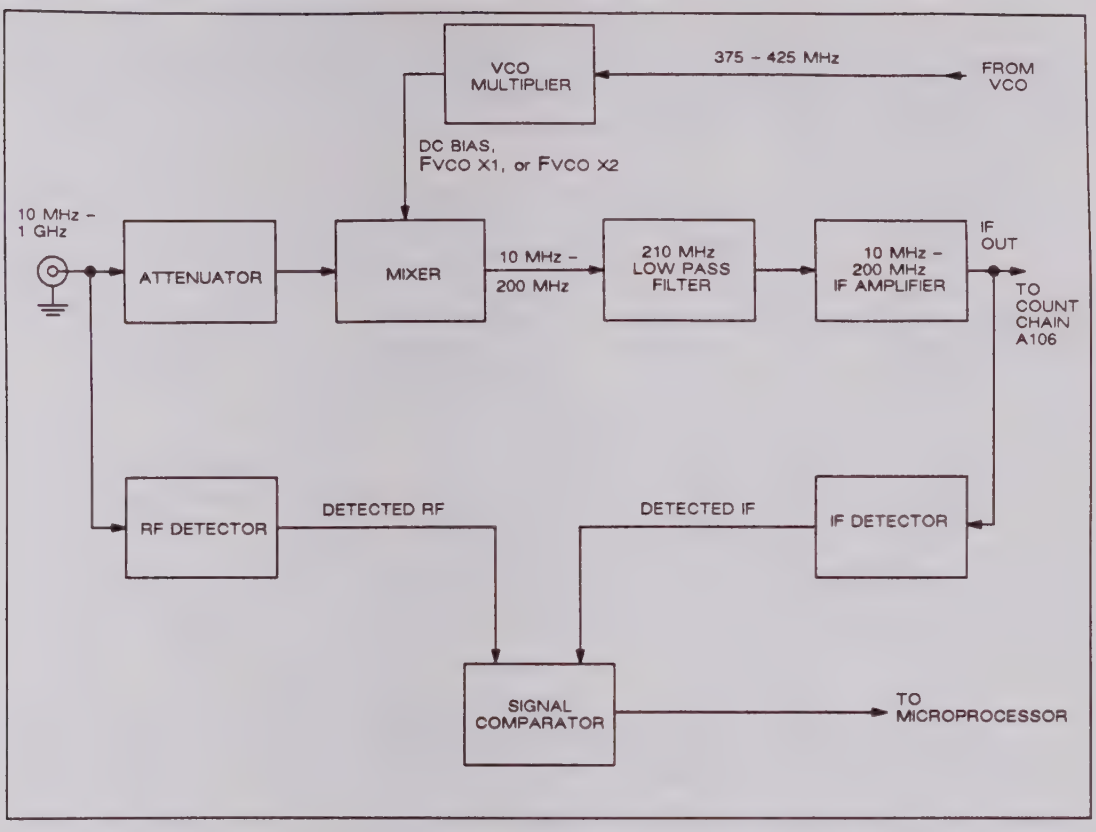


Figure 4-2. Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as FIN = N FVCO ± FIF. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and FVCO and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the ± sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in Figure 4-3.

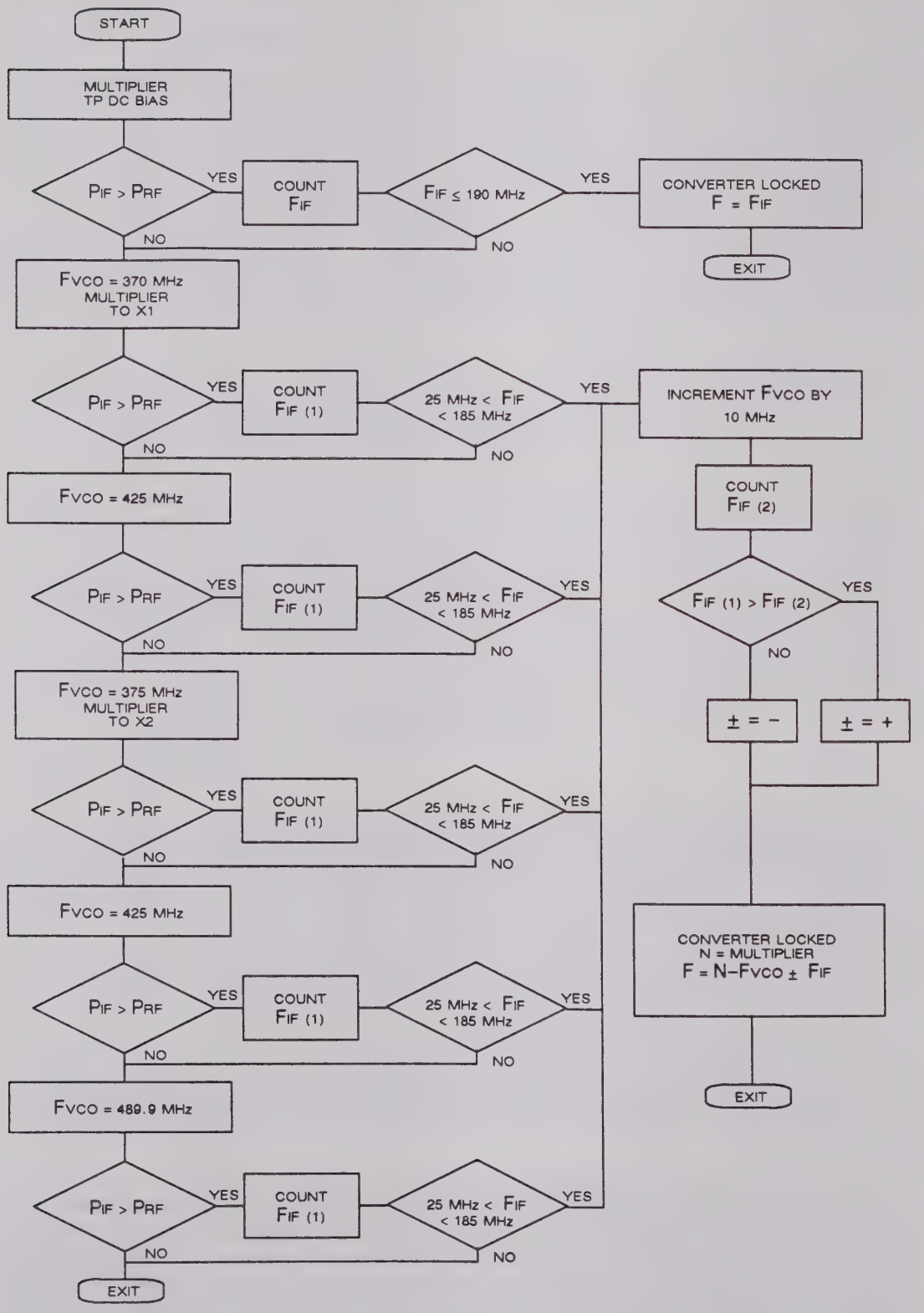


Figure 4-3. Band 2 Converter Operation

The L.O. frequencies being used, except the range of direct counting (<190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range FIN (MHz)	VCO Frequency FVCO (MHz)	Harmonic Number N	IF Frequency Range FIF (MHz)
10 – 190	–	0	10 – 190
185 – 345	370	1	185 – 25
345 – 400	425	1	80 – 25
400 – 560	375	1	25 – 185
560 – 610	425	1	135 – 185
610 – 725	375	2	140 – 25
725 – 825	425	2	125 – 25
825 – 935	375	2	75 – 185
935 – 1035	425	2	85 – 185
1035 – 1164.8	489.9	2	55.2 – 185

Figure 4-4. Band 2 Operating Ranges

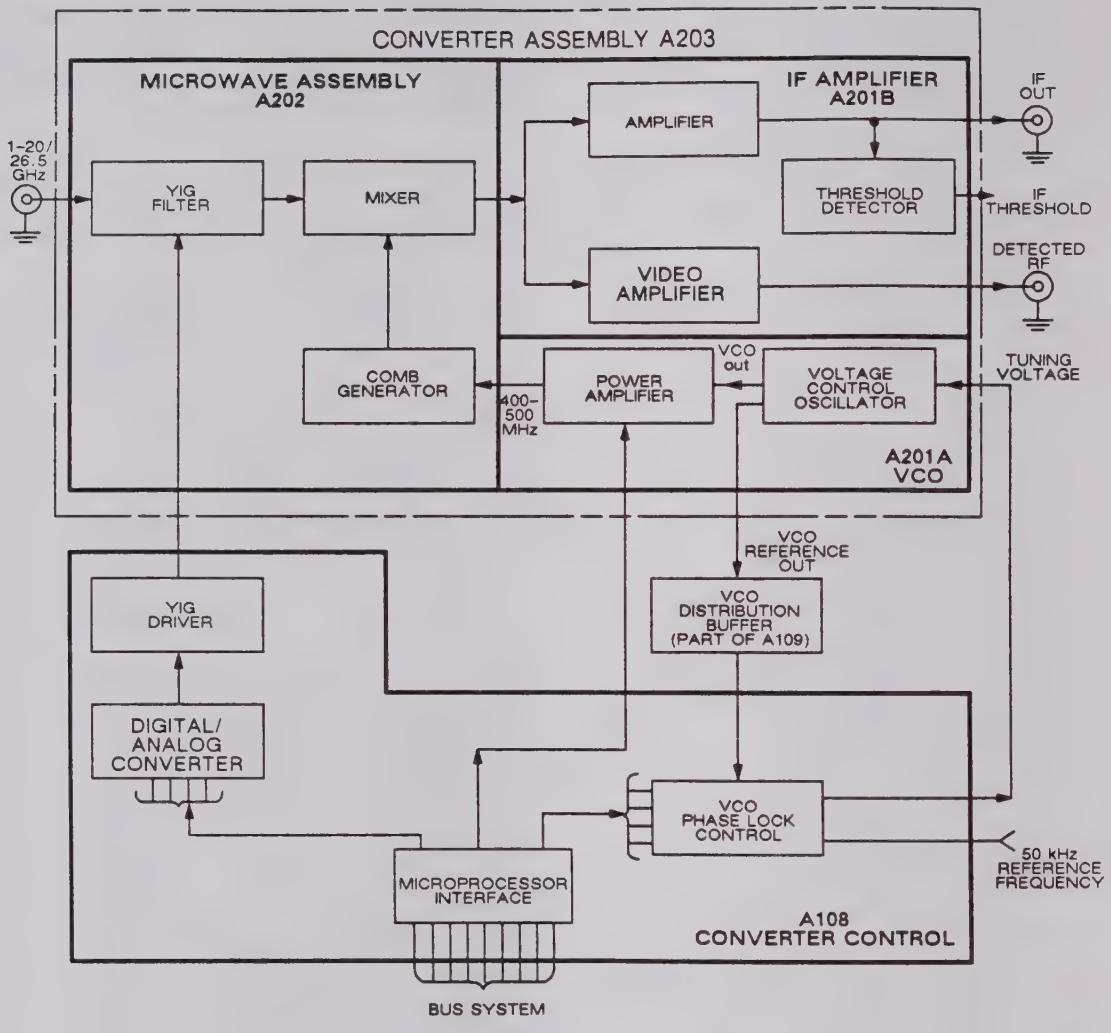


Figure 4-5. Band 3 Converter, Simplified

BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 127 MHz. This is accomplished by mixing the input signal with a known reference frequency, which is found by selecting a VCO harmonic in the range of 400 to 500 MHz. The VCO frequency can be selected in 50 kHz increments by using a microprocessor controlled phase lock system, while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in Figure 4-5. There are two major assemblies. The Converter Control Assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control Assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current (YIG) driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) Assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (YIG)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz – 20 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly.

The output of the video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

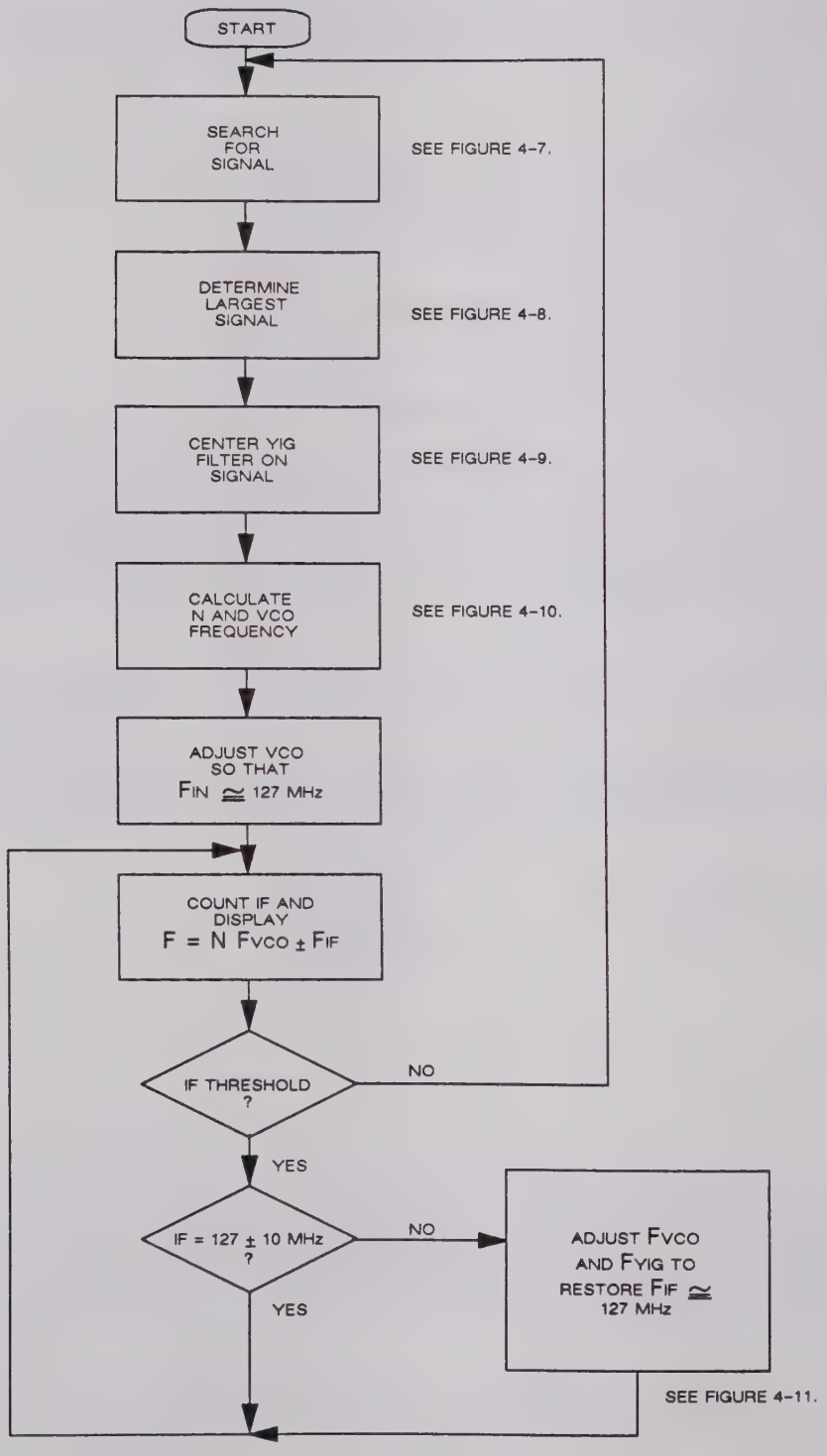


Figure 4-6. Band 3 Operation, Simplified

On units equipped with the Power Measurement Option (02), accurate frequency correction factors are stored in the counter's memory. This allows absolute power calibration of the video amplifier output.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 127 MHz. An approximation of the input signal is found by using:

$$F_{IN} = N F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the Count Chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped, (in 64 MHz steps), from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figure 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down (in 2 MHz increments) until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} - 127}{500}$ and then rounded up to the next highest integer.

From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} - 127}{N}$. Should this yield $F_{VCO} < 400$ MHz, then

F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} + 127}{N}$.

Since F_{YIG} is only approximately equal to F_{IF}, the IF frequency will not be exactly 127 MHz. Therefore, the next step in operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{YIG} - 127}{N}$. If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in $\pm$ 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 127 MHz. This method provides rapid tracking of a signal being tuned.

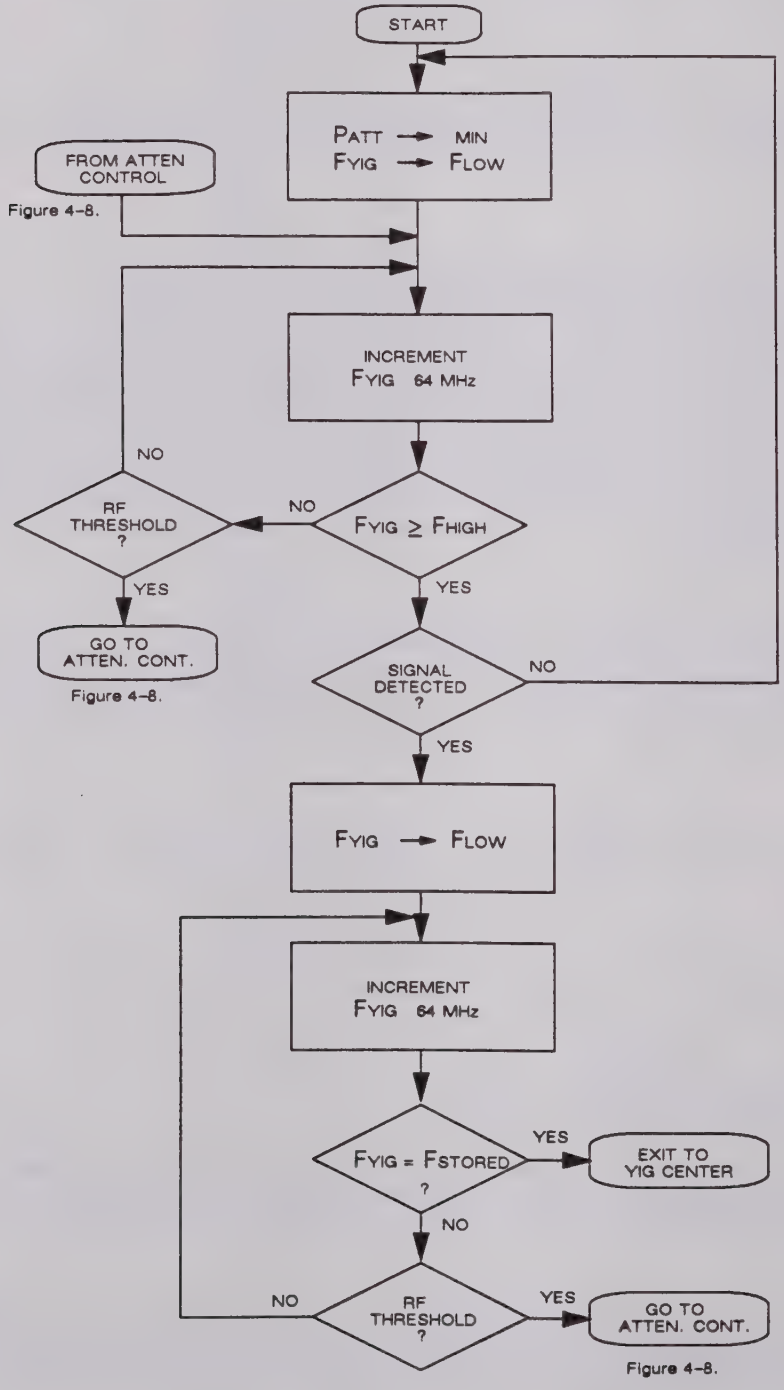


Figure 4-7. Band 3 Search For Signal

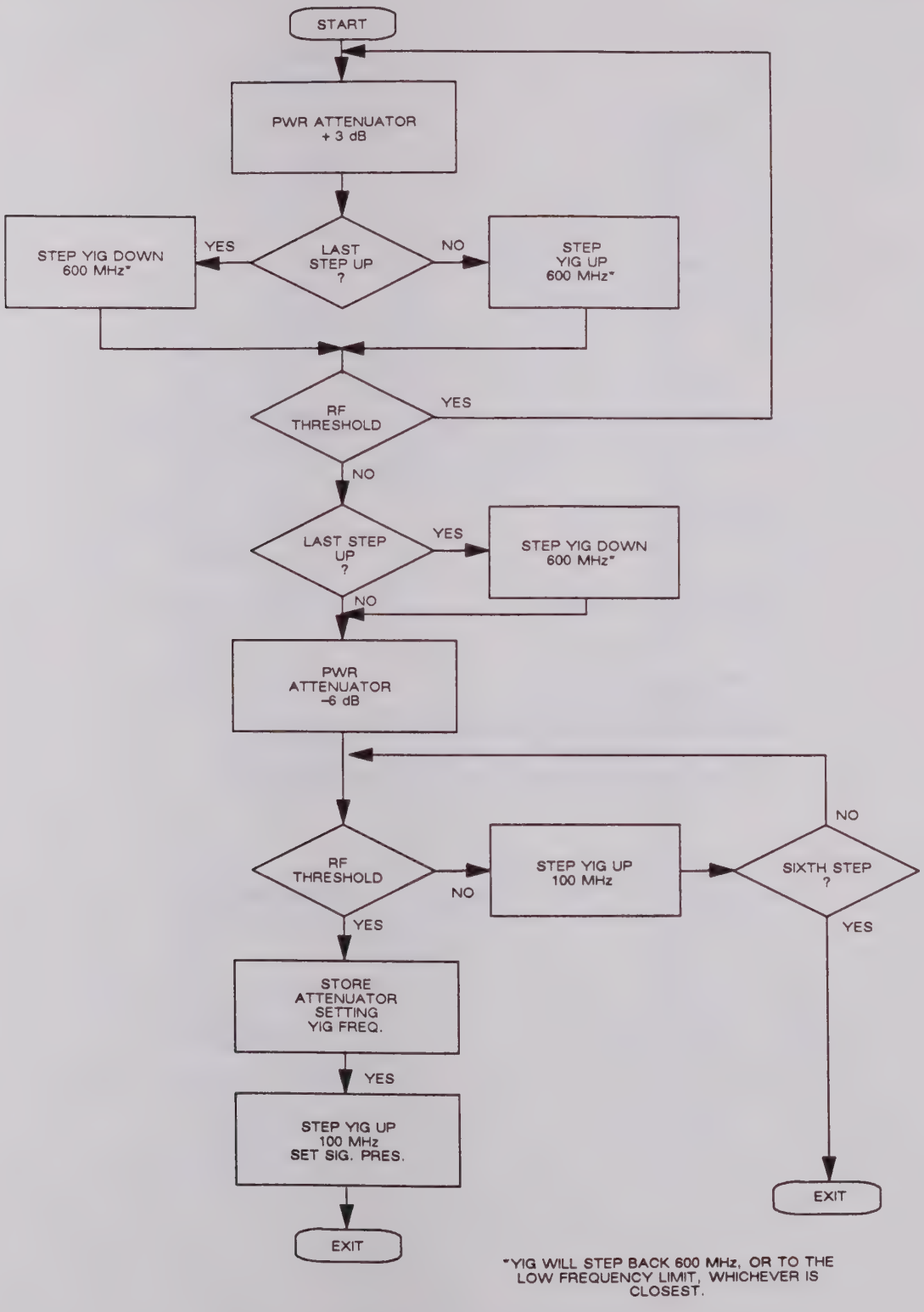


Figure 4-8. Determine Largest Signal (Attenuator Count)

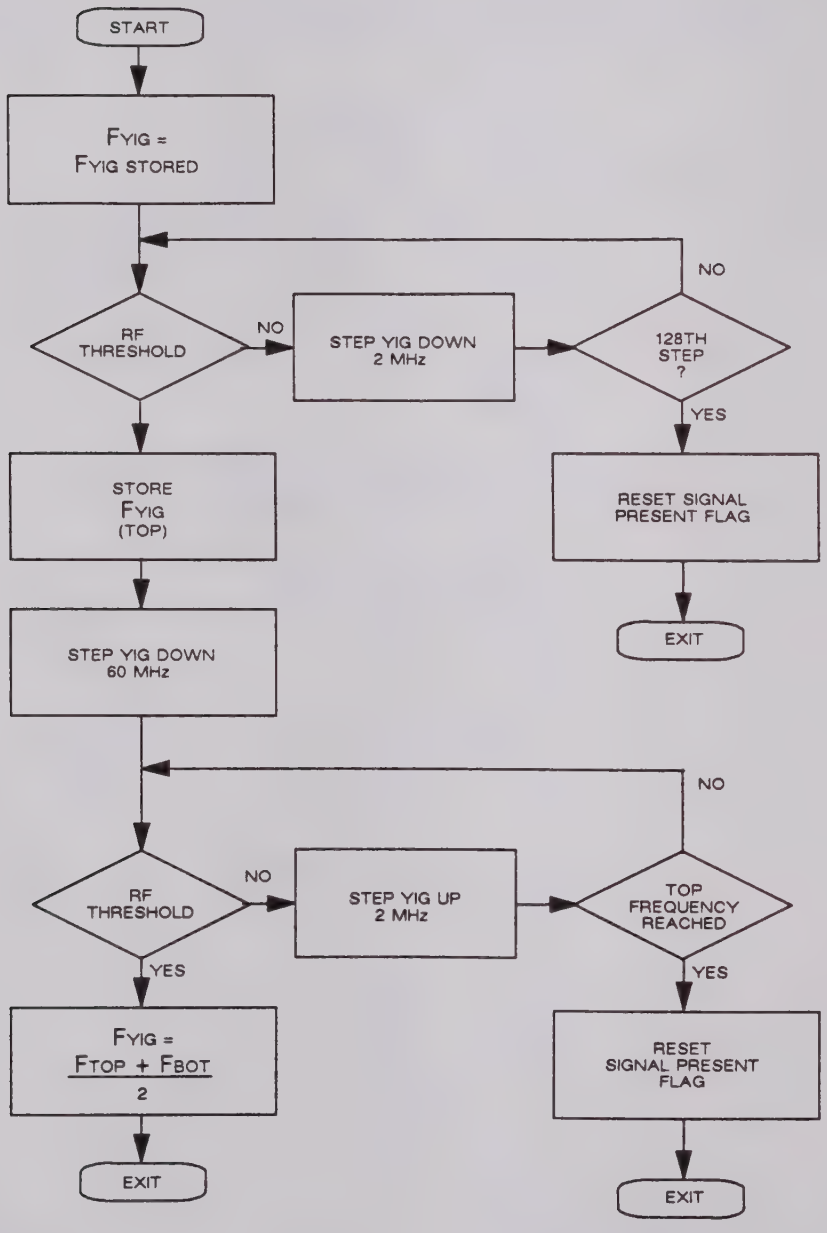


Figure 4-9. YIG Centering

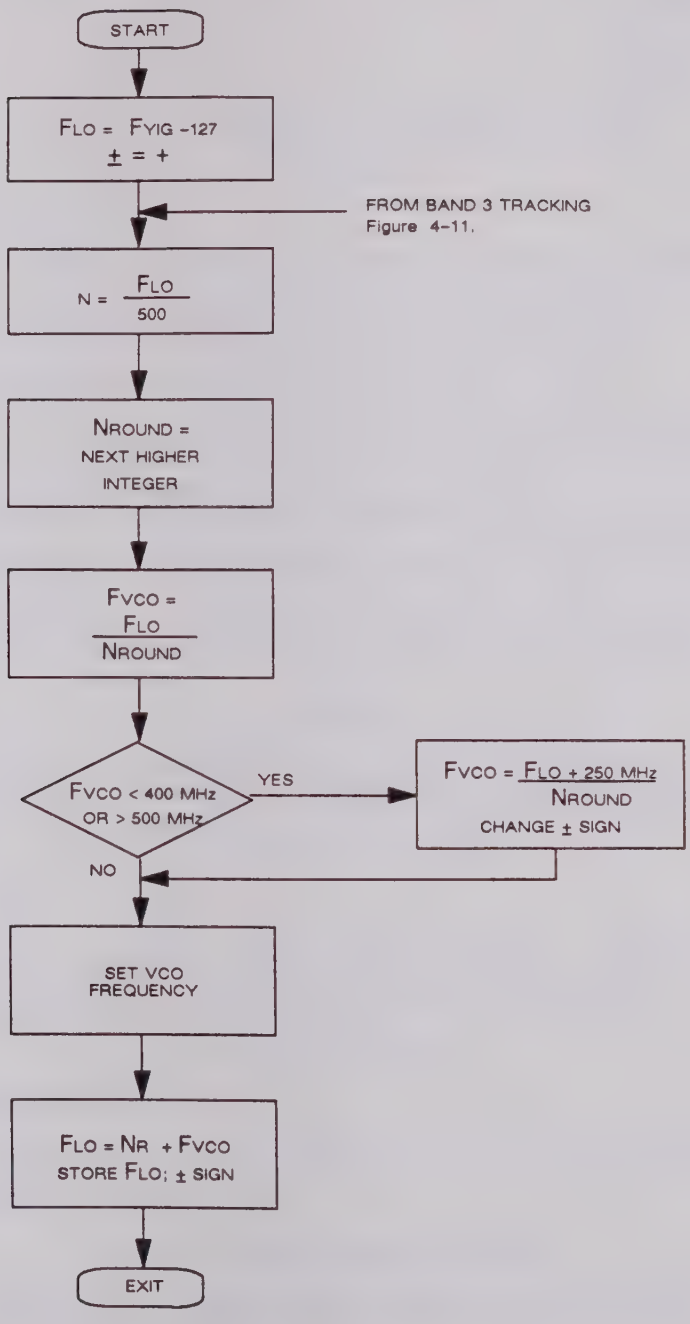


Figure 4-10. Calculate VCO and N Frequency

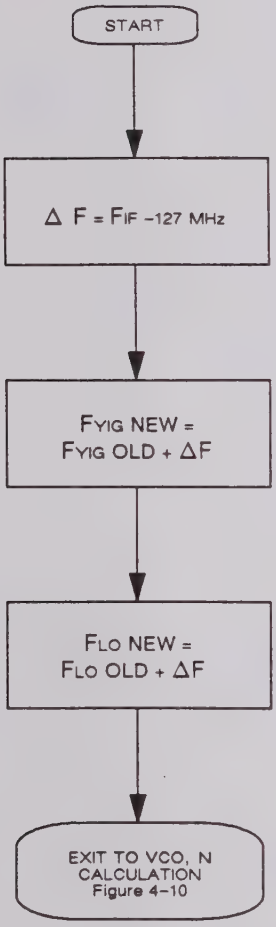


Figure 4–11. Band 3 Signal Tracking

Section 5
Maintenance and Service

This section contains instructions and information to maintain your counter.

FUSE REPLACEMENT

The counter uses one fuse. It is located on the rear panel next to the voltage select switch.

- For 100/120 Vac operation use a 1.0A slow-blow MDL-type fuse.
- For 220/240 Vac operation use a 0.50A slow-blow FST-type fuse.

The voltage select switch should be set to the proper line voltage. To change line voltage:

1. Be sure the counter is disconnected from the power line.
2. With a flat edged screwdriver, rotate the voltage select switch until the arrow points to the desired line voltage.
3. Change to a fuse with the value specified for the line voltage selected.

NOTE

Always be sure that the fuse is the type and value specified for, and that the voltage select switch is set to correspond to the AC power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce counter stability and shorten component life.

PERIODIC MAINTENANCE

No periodic maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

CAUTION

Do not attempt repair or disassembly of the Microwave Converter or Time Base Oscillator Assemblies. Contact EIP or your sales representative.

If the following assemblies are repaired or replaced, the counter may require recalibration for proper operation.

- Power Supply (A101)
- Microprocesor (A105)
- Gate Generator (A107)
- Converter Control (A108)
- Microwave Converter (A203)

Care should be taken when removing any assemblies to prevent damage to components or cables.

FACTORY SERVICE

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

1. Name and address of owner.
2. Model and complete serial number of counter.
3. A COMPLETE description of the problem (Under what conditions did the problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptoms?).
4. Name and telephone number of someone familiar with the problem who may be contacted by EIP for further information, if necessary.
5. Shipping address to which the counter is to be returned. Include any special shipping instructions.
6. Pack the counter for shipping (Refer to Section 2).

FIELD SERVICE

EIP has an assembly exchange program. Selected plug-in assemblies and modules may be exchanged. Consult with the factory for the current listing.

Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 545B/548B counter. They are:

- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SELF DIAGNOSTICS

At turn-on, the counter performs several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests it then enters the normal operating mode. If it fails RAM check, the display will show all Es. If the counter fails any of the PROM checks, an error message will be displayed. Please refer to Figure 6-1.

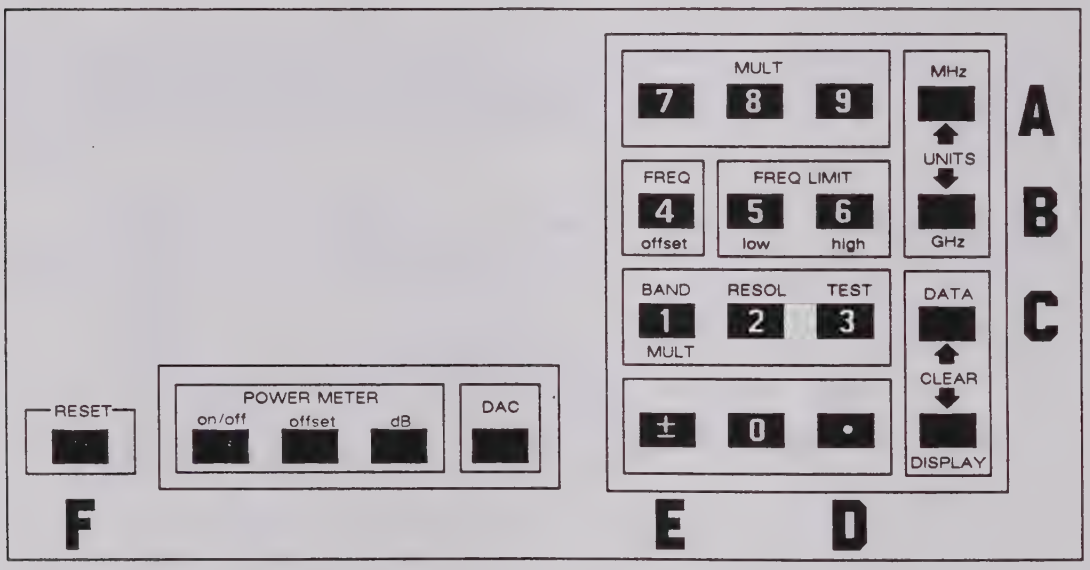
The counter generates PROM error signatures only during the power up diagnostics check. It is necessary to turn the power off, and then on again, while the signature analyzer is connected, to get a signature.

PROBLEM	ERROR
RAM Bad	All E's
A105 U11 (Basic Program) Bad	31
A105 U12 (Basic Program) Bad	32
A105 U13 (Basic Program) Bad	33

Figure 6-1. Self Diagnostic Error Indications

KEYBOARD CONTROLLED CIRCUIT TESTS

There are 11 keyboard controlled circuit tests (01 thru 11). All tests are accessed by pressing TEST and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07, 11) can be exited by pressing any key. The counter will exit the test and enter the function selected. Tests which use the keyboard in their operation (tests 05, 08, 09, 10) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR DISPLAY. The counter will return to normal operation. Some tests require hexidecimal coded keyboard inputs (tests 08, 09, 10). For those tests the keyboard is defined in Figure 6-2.



KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	•	D
6	6	±	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-2. Keyboard Configuration For Tests Requiring Hexadecimal Inputs.

TESTS

01 **200 MHz Self Test.** This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **8's Test.** This will light all LEDs, annunciators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LEDs and annunciators.

03 **Display Segment Test.** This lights one segment of each digit, and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers and display multiplexer operate properly and independently.

04 **Display Digit Test.** This lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 **Keyboard Test.** This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so the keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to TP5. This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry.

06 **Converter Ramp Test.** Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB) steps. It can be used to test the YIG DAC, YIG drivers, YIG, and Band 3 RF level circuits.

07 **VCO Test.** This test cycles the VCO frequency from 400 to 500 MHz, in increments of 50 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry.

08 **Power Meter Offset Test.** This makes it possible to set the power meter zero DAC to any setting. The setting is entered as a four digit hexidecimal number. The first two digits are used to program the coarse offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in testing the power meter circuit.

09 **Power Meter Gain Test.** This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexidecimal number in the following format.

1st digit	A107 U10 bits 4–7
2nd digit	A107 U10 bits 0–3
3rd digit	A107 U12 bits 4–7 (Power Meter Option only)
4th digit	A107 U12 bits 0–3 (Power Meter Option only)
5th digit bit 0	Sets Amp marker "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marker "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0–3. Tests 09 checks the RF level and power meter circuits.

10 **Information Read/Alter Routine.** Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexidecimal number. When the 4th digit is entered, the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexidecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation, turn the counter off then back on.

11 Test 11 for the DAC Option 01 is described in Section 10.

SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on DAC Board (A103)	A820	A822
PIA on Count Chain (A106)	2C00	2602
PIA on Gate Generator (A107)	1900	1902
Frequency Control PIA on Converter Control (A108)	1840	1842
Programmable Counter PIA on Converter Control (A108)	1820	1822
PIA on Band 2 Converter (A109)	1880	1882
PIA on Front Panel Logic (A111)	1808	180A

DESCRIPTION	ADDRESS
GPIB Address Switch	1C04

Figure 6-3. I/O Addresses

Two important I/O port locations are the YIG frequency control (address 1840, 1842) and the VCO frequency control (address 1820, 1822).

To convert from the desired YIG frequency to the PIA program number:

1. Round the desired frequency to a multiple of 2 MHz (The YIG DAC resolution is 2 MHz).
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexidecimal.
4. The two most significant digits are programmed to address 1842, and the two least significant digits are programmed to address 1840.

To convert from the desired VCO frequency to the PIA program number:

EXAMPLE (420.75 MHz)

1. Round the desired frequency to a multiple of 50 kHz (The resolution of the VCO frequency is 50 kHz).
2. Multiply the desired frequency (in MHz) by 5 ..... 420.75 X 5 = 2103.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 ..... 75 X 16 = 12
5. Add the result to the most significant digit from step 2 ..... MSD of 2103.75 = 2 – 2 + 12 = 14
6. Convert the result to hexidecimal ..... $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part ..... 2103.75 → E103
8. The two most significant digits are programmed to address 1822, and the two least significant digits are programmed to address 1820.

SIGNIFICANT ADDRESSES, RAM

All storage in RAM are in the following formats.

REGISTER FORMAT, FREQUENCY STORAGE			REGISTER FORMAT, POWER STORAGE		
ADDRESS	SIGN (00 = +, FF = –)		ADDRESS	SIGN (00 = +, FF = –)	
ADDRESS + 1	100 GHz	10 GHz	ADDRESS + 1	NOT USED	
ADDRESS + 2	1 GHz	100 MHz	ADDRESS + 2	NOT USED	
ADDRESS + 3	10 MHz	1 MHz	ADDRESS + 3	NOT USED	
ADDRESS + 4	100 kHz	10 kHz	ADDRESS + 4	NOT USED	
ADDRESS + 5	1 kHz	100 Hz	ADDRESS + 5	100 dB	10 dB
ADDRESS + 6	10 Hz	1 Hz	ADDRESS + 6	1 dB	.1 dB

REGISTER	ADDRESS
L.O. Frequency	01A8
I.F. Frequency	023F
Frequency output to display	01B8
Frequency limit low	025B
Frequency limit high	0254
Frequency offset	0246

Figure 6-4. Frequency Storage Registers

REGISTER	ADDRESS
Power output to display	01BF
Power offset	024D

Figure 6-5. Power Storage Registers

TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- Power Supply (A101)
- Microprocessor (A105)
- Gate Generator (A107)
- Converter Control (A108)
- Converter Assembly (A203)

CAUTION

Do not attempt to repair or disassemble the A203 hybrid assembly.

TEST EQUIPMENT REQUIRED

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	127 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz – 10 MHz
Wavetek	2002	Sweeper	10 MHz – 2 GHz
EIP	931	Microwave Sweeper	1 GHz – 18.6 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz – 26.5 GHz

Figure 6-6. Troubleshooting Test Equipment (Or Equivalent).

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.
2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.
3. Refer to the appropriate troubleshooting tree for the failure mode.

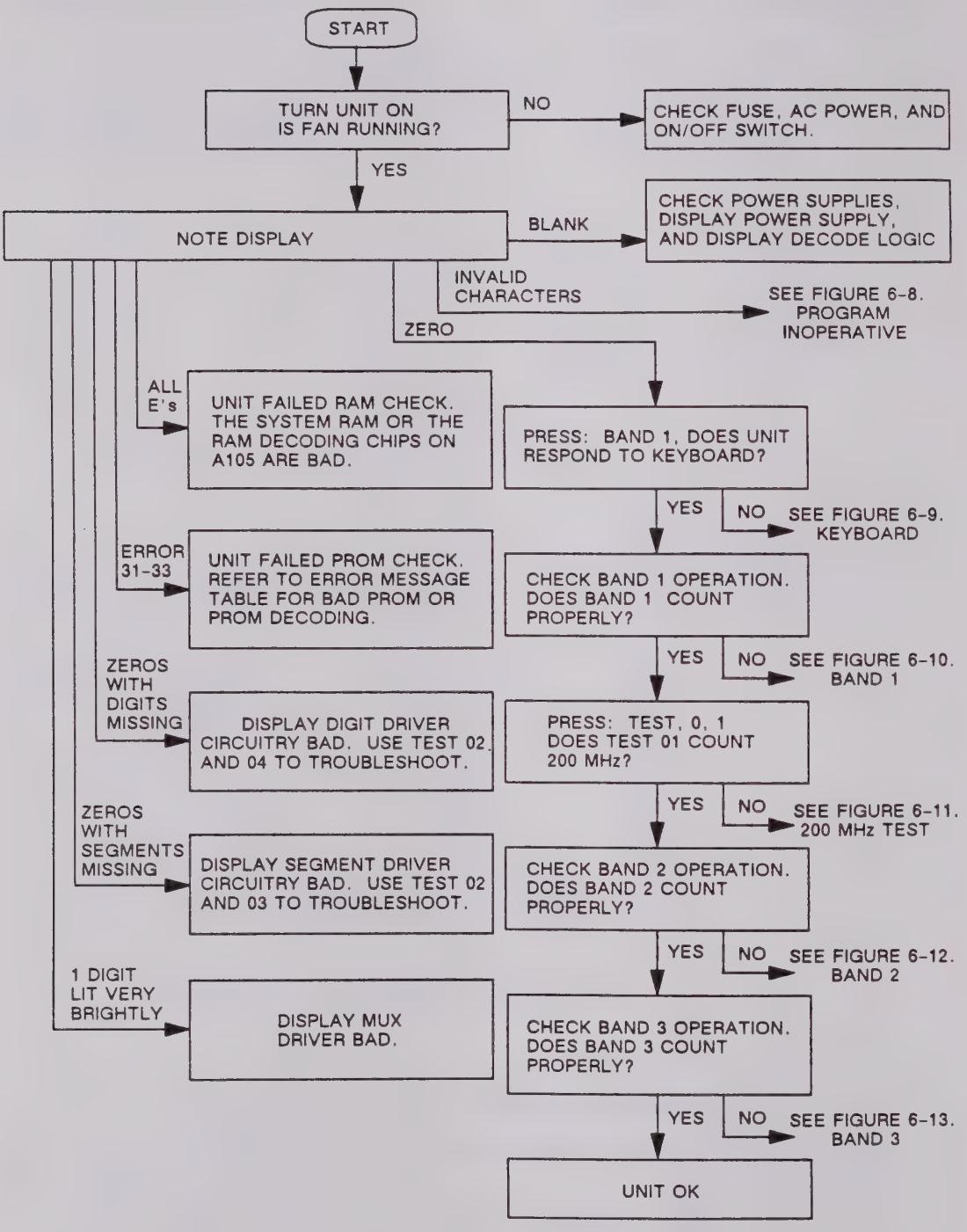

START
TURN UNIT ON
IS FAN RUNNING?
NO
CHECK FUSE, AC POWER, AND ON/OFF SWITCH.
YES
NOTE DISPLAY
BLANK
CHECK POWER SUPPLIES, DISPLAY POWER SUPPLY, AND DISPLAY DECODE LOGIC
INVALID CHARACTERS
SEE FIGURE 6-8. PROGRAM INOPERATIVE
ZERO
ALL E's
UNIT FAILED RAM CHECK. THE SYSTEM RAM OR THE RAM DECODING CHIPS ON A105 ARE BAD.
PRESS: BAND 1, DOES UNIT RESPOND TO KEYBOARD?
YES
NO
SEE FIGURE 6-9. KEYBOARD
ERROR 31-33
UNIT FAILED PROM CHECK. REFER TO ERROR MESSAGE TABLE FOR BAD PROM OR PROM DECODING.
CHECK BAND 1 OPERATION. DOES BAND 1 COUNT PROPERLY?
YES
NO
SEE FIGURE 6-10. BAND 1
ZEROS WITH DIGITS MISSING
DISPLAY DIGIT DRIVER CIRCUITRY BAD. USE TEST 02 AND 04 TO TROUBLESHOOT.
PRESS: TEST, 0, 1 DOES TEST 01 COUNT 200 MHz?
YES
NO
SEE FIGURE 6-11. 200 MHz TEST
ZEROS WITH SEGMENTS MISSING
DISPLAY SEGMENT DRIVER CIRCUITRY BAD. USE TEST 02 AND 03 TO TROUBLESHOOT.
CHECK BAND 2 OPERATION. DOES BAND 2 COUNT PROPERLY?
YES
NO
SEE FIGURE 6-12. BAND 2
1 DIGIT LIT VERY BRIGHTLY
DISPLAY MUX DRIVER BAD.
CHECK BAND 3 OPERATION. DOES BAND 3 COUNT PROPERLY?
YES
NO
SEE FIGURE 6-13. BAND 3
UNIT OK

Figure 6-7. Main Troubleshooting Tree

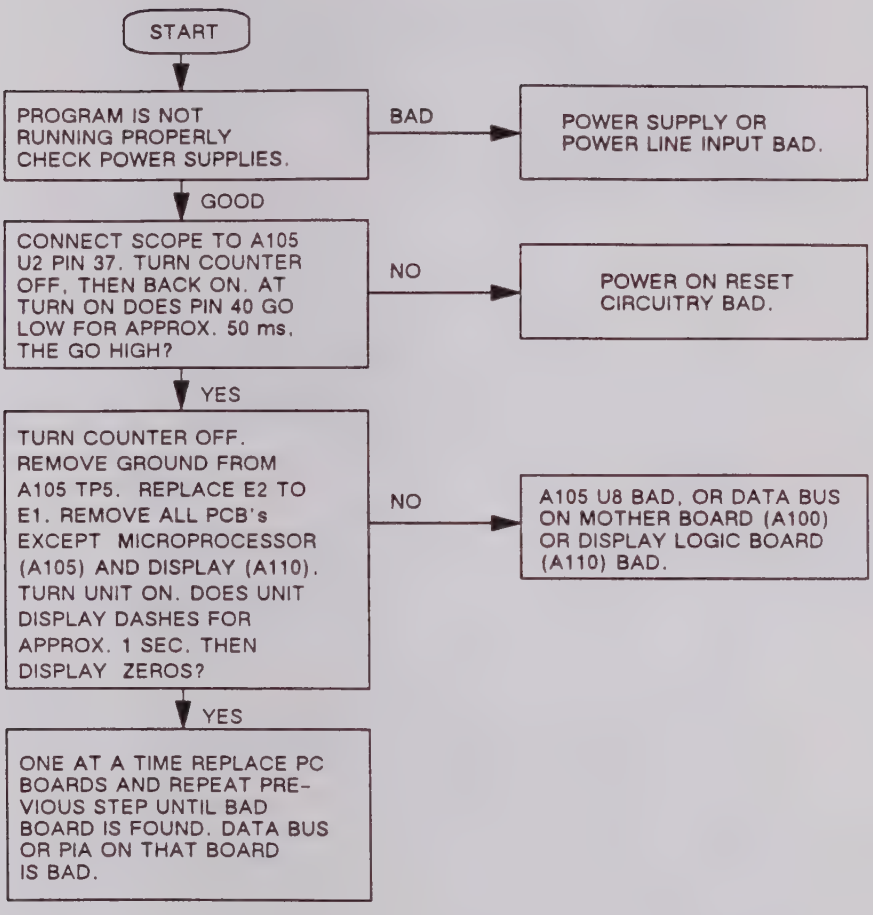

START
PROGRAM IS NOT RUNNING PROPERLY CHECK POWER SUPPLIES.
BAD
POWER SUPPLY OR POWER LINE INPUT BAD.
GOOD
CONNECT SCOPE TO A105 U2 PIN 37. TURN COUNTER OFF, THEN BACK ON. AT TURN ON DOES PIN 40 GO LOW FOR APPROX. 50 ms. THE GO HIGH?
NO
POWER ON RESET CIRCUITRY BAD.
YES
TURN COUNTER OFF. REMOVE GROUND FROM A105 TP5. REPLACE E2 TO E1. REMOVE ALL PCB's EXCEPT MICROPROCESSOR (A105) AND DISPLAY (A110). TURN UNIT ON. DOES UNIT DISPLAY DASHES FOR APPROX. 1 SEC. THEN DISPLAY ZEROS?
NO
A105 U8 BAD, OR DATA BUS ON MOTHER BOARD (A100) OR DISPLAY LOGIC BOARD (A110) BAD.
YES
ONE AT A TIME REPLACE PC BOARDS AND REPEAT PREVIOUS STEP UNTIL BAD BOARD IS FOUND. DATA BUS OR PIA ON THAT BOARD IS BAD.

Figure 6-8. Program Inoperative

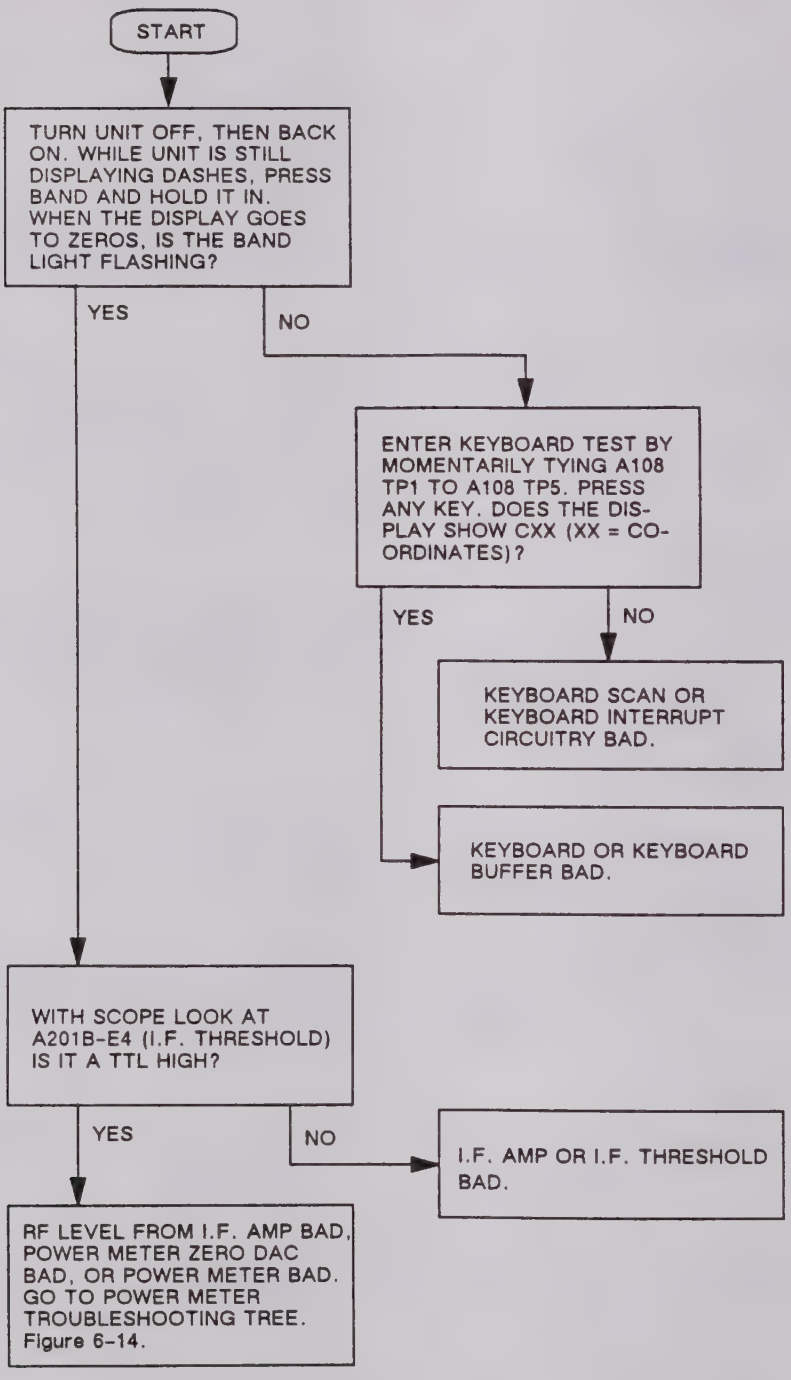

START
TURN UNIT OFF, THEN BACK ON. WHILE UNIT IS STILL DISPLAYING DASHES, PRESS BAND AND HOLD IT IN. WHEN THE DISPLAY GOES TO ZEROS, IS THE BAND LIGHT FLASHING?
YES
NO
ENTER KEYBOARD TEST BY MOMENTARILY TYING A108 TP1 TO A108 TP5. PRESS ANY KEY. DOES THE DISPLAY SHOW CXX (XX = COORDINATES)?
YES
NO
KEYBOARD SCAN OR KEYBOARD INTERRUPT CIRCUITRY BAD.
KEYBOARD OR KEYBOARD BUFFER BAD.
WITH SCOPE LOOK AT A201B-E4 (I.F. THRESHOLD) IS IT A TTL HIGH?
YES
NO
I.F. AMP OR I.F. THRESHOLD BAD.
RF LEVEL FROM I.F. AMP BAD, POWER METER ZERO DAC BAD, OR POWER METER BAD. GO TO POWER METER TROUBLESHOOTING TREE. Figure 6-14.

Figure 6-9. Keyboard

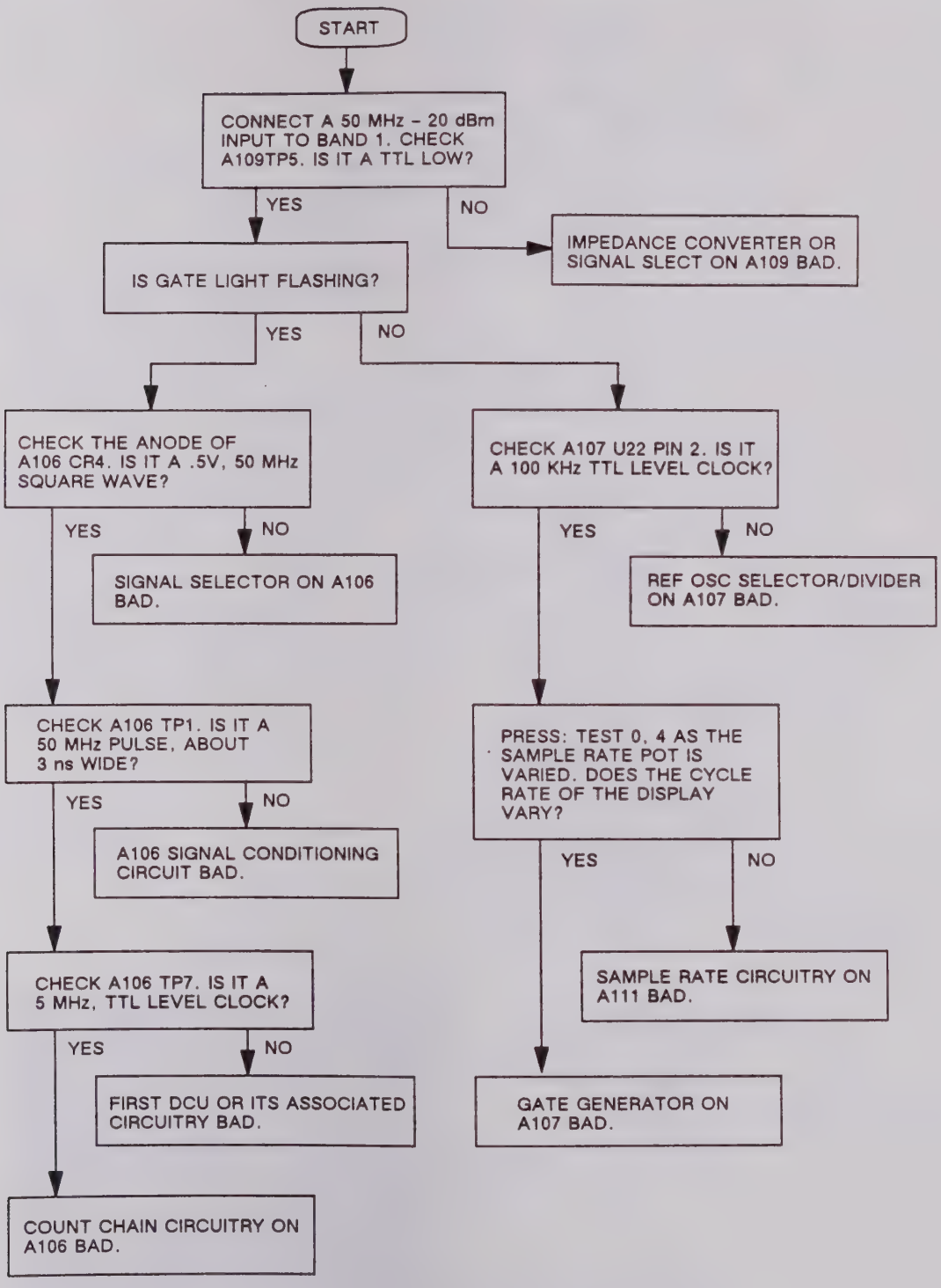

START
CONNECT A 50 MHz - 20 dBm INPUT TO BAND 1. CHECK A109TP5. IS IT A TTL LOW?
YES
NO
IMPEDANCE CONVERTER OR SIGNAL SLECT ON A109 BAD.
IS GATE LIGHT FLASHING?
YES
NO
CHECK THE ANODE OF A106 CR4. IS IT A .5V, 50 MHz SQUARE WAVE?
CHECK A107 U22 PIN 2. IS IT A 100 KHz TTL LEVEL CLOCK?
YES
NO
SIGNAL SELECTOR ON A106 BAD.
YES
NO
REF OSC SELECTOR/DIVIDER ON A107 BAD.
CHECK A106 TP1. IS IT A 50 MHz PULSE, ABOUT 3 ns WIDE?
PRESS: TEST 0, 4 AS THE SAMPLE RATE POT IS VARIED. DOES THE CYCLE RATE OF THE DISPLAY VARY?
YES
NO
A106 SIGNAL CONDITIONING CIRCUIT BAD.
YES
NO
SAMPLE RATE CIRCUITRY ON A111 BAD.
CHECK A106 TP7. IS IT A 5 MHz, TTL LEVEL CLOCK?
YES
NO
FIRST DCU OR ITS ASSOCIATED CIRCUITRY BAD.
GATE GENERATOR ON A107 BAD.
COUNT CHAIN CIRCUITRY ON A106 BAD.

Figure 6-10. Band 1

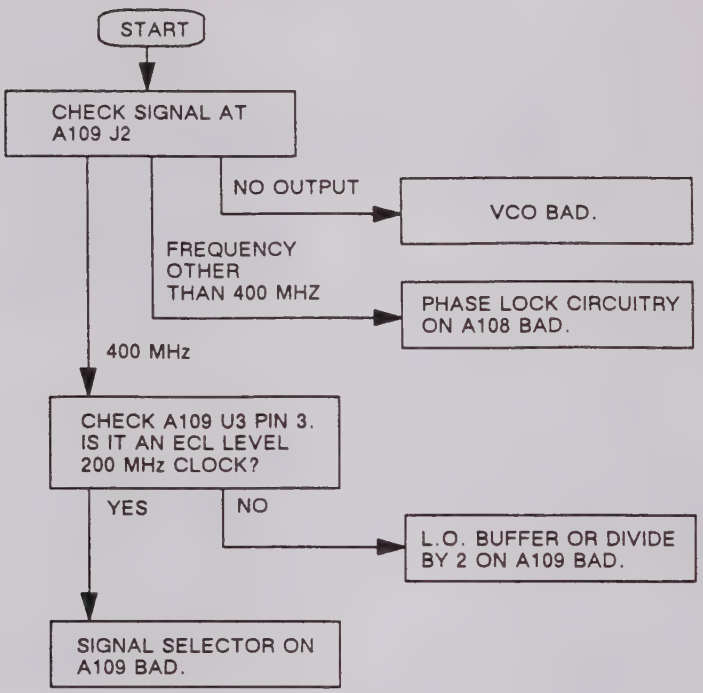

START
CHECK SIGNAL AT A109 J2
NO OUTPUT
VCO BAD.
FREQUENCY OTHER THAN 400 MHZ
PHASE LOCK CIRCUITRY ON A108 BAD.
400 MHz
CHECK A109 U3 PIN 3. IS IT AN ECL LEVEL 200 MHz CLOCK?
YES
NO
L.O. BUFFER OR DIVIDE BY 2 ON A109 BAD.
SIGNAL SELECTOR ON A109 BAD.

Figure 6-11. 200 MHz Test

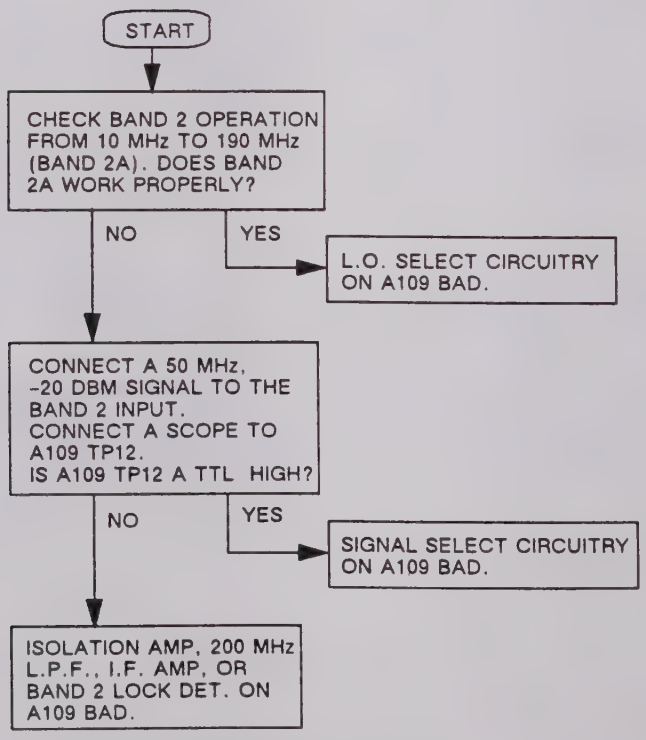

START
CHECK BAND 2 OPERATION FROM 10 MHz TO 190 MHz (BAND 2A). DOES BAND 2A WORK PROPERLY?
NO
YES
L.O. SELECT CIRCUITRY ON A109 BAD.
CONNECT A 50 MHz, -20 DBM SIGNAL TO THE BAND 2 INPUT. CONNECT A SCOPE TO A109 TP12. IS A109 TP12 A TTL HIGH?
NO
YES
SIGNAL SELECT CIRCUITRY ON A109 BAD.
ISOLATION AMP, 200 MHz L.P.F., I.F. AMP, OR BAND 2 LOCK DET. ON A109 BAD.

Figure 6-12. Band 2

START

WHAT IS SYMPTOM OF BAND 3 PROBLEM?

UNIT COUNTS WRONG NUMBER

VCO IS GENERATING WRONG FREQUENCY. CONNECT CONVERTER TO A109 J2. (VCO REF.) IS FREQUENCY BETWEEN 400 MHz AND 500 MHz? AND STABLE?

YES

Ø LOCK CIRCUITRY ON A108 BAD.

NO

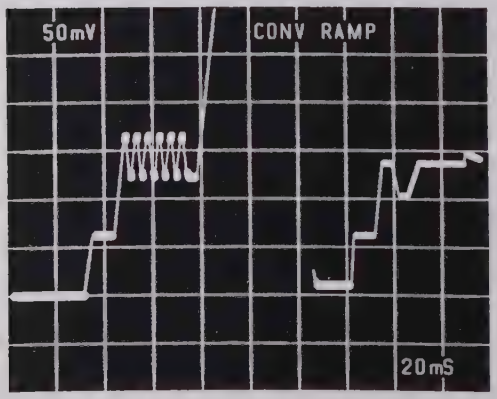
VCO NOT Ø LOCKED. CONNECT A POWER SUPPLY TO A201 J3. VARY VOLTAGE FROM 1 TO 10V. DOES THE VCO FREQUENCY VARY FROM APPROX. 370 MHz TO APPROX. 510 MHz?

YES

Ø LOCK CIRCUITRY ON A108 BAD.

NO

VCO BAD



UNIT COUNTS AFTER SIGNAL IS REMOVED

I.F. THRESHOLD BAD

UNIT DOES NOT COUNT

WITH NO SIGNAL INTO THE COUNTER, CONNECT A SCOPE TO A100J7 PIN 2. DOES IT CONTAIN A 60 ms RAMP?

YES

NO

B

CONNECT A SIGNAL WITHIN THE OPERATING RANGE OF BAND 3 TO THE BAND 3 INPUT. WITH A SCOPE LOOK AT A100J7 PIN 2. IT SHOULD CONTAIN A COMPLEX WAVEFORM. DOES A PORTION OF THE WAVEFORM LOOK LIKE THE WAVEFORM SHOWN IN THE LOWER LEFT?

NO

YES

A

POWER METER OR POWER METER ZERO CIRCUITS ON A107 BAD.

SEE FIGURE 6-14. POWER METER

Figure 6-13. Band 3

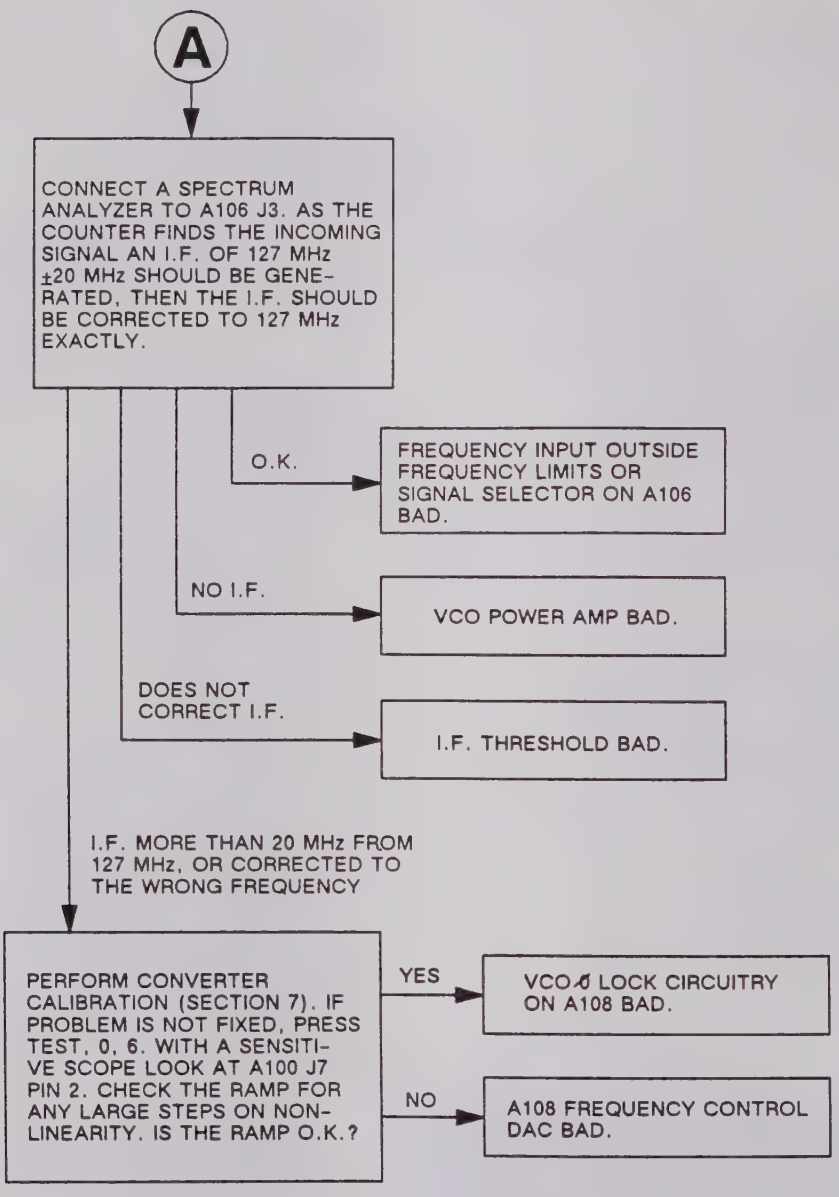

A
CONNECT A SPECTRUM ANALYZER TO A106 J3. AS THE COUNTER FINDS THE INCOMING SIGNAL AN I.F. OF 127 MHz ±20 MHz SHOULD BE GENERATED, THEN THE I.F. SHOULD BE CORRECTED TO 127 MHz EXACTLY.
O.K.
FREQUENCY INPUT OUTSIDE FREQUENCY LIMITS OR SIGNAL SELECTOR ON A106 BAD.
NO I.F.
VCO POWER AMP BAD.
DOES NOT CORRECT I.F.
I.F. THRESHOLD BAD.
I.F. MORE THAN 20 MHz FROM 127 MHz, OR CORRECTED TO THE WRONG FREQUENCY
PERFORM CONVERTER CALIBRATION (SECTION 7). IF PROBLEM IS NOT FIXED, PRESS TEST, 0, 6. WITH A SENSITIVE SCOPE LOOK AT A100 J7 PIN 2. CHECK THE RAMP FOR ANY LARGE STEPS ON NON-LINEARITY. IS THE RAMP O.K.?
YES
VCO Ø LOCK CIRCUITRY ON A108 BAD.
NO
A108 FREQUENCY CONTROL DAC BAD.

Figure 6-13. Band 3, Continued

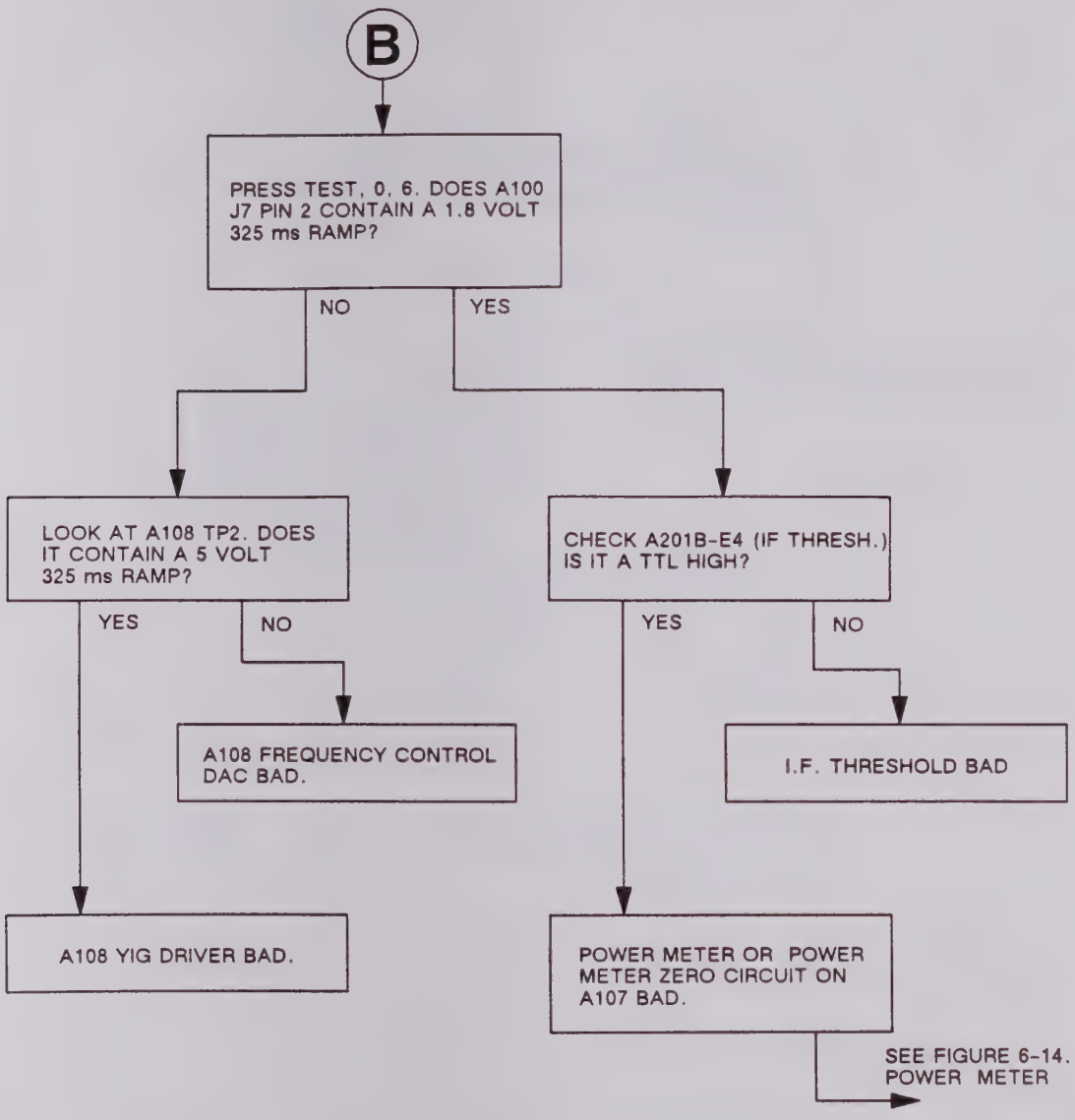

B
PRESS TEST, 0, 6. DOES A100 J7 PIN 2 CONTAIN A 1.8 VOLT 325 ms RAMP?
NO
YES
LOOK AT A108 TP2. DOES IT CONTAIN A 5 VOLT 325 ms RAMP?
YES
NO
A108 FREQUENCY CONTROL DAC BAD.
A108 YIG DRIVER BAD.
CHECK A201B-E4 (IF THRESH.) IS IT A TTL HIGH?
YES
NO
I.F. THRESHOLD BAD
POWER METER OR POWER METER ZERO CIRCUIT ON A107 BAD.
SEE FIGURE 6-14. POWER METER

Figure 6-13. Band 3, Continued

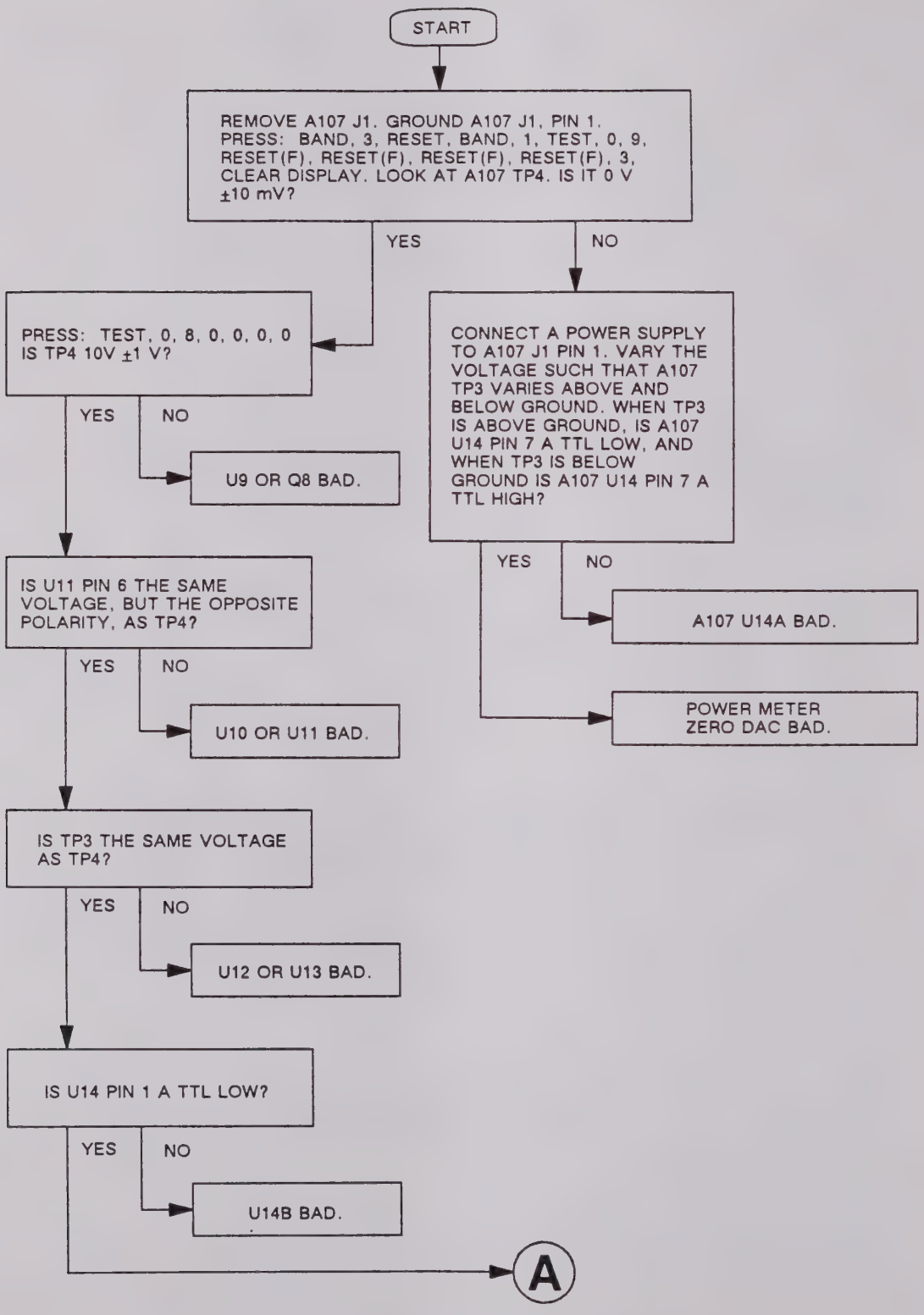

START
REMOVE A107 J1. GROUND A107 J1, PIN 1. PRESS: BAND, 3, RESET, BAND, 1, TEST, 0, 9, RESET(F), RESET(F), RESET(F), RESET(F), 3, CLEAR DISPLAY. LOOK AT A107 TP4. IS IT 0 V ±10 mV?
YES
NO
PRESS: TEST, 0, 8, 0, 0, 0, 0 IS TP4 10V ±1 V?
CONNECT A POWER SUPPLY TO A107 J1 PIN 1. VARY THE VOLTAGE SUCH THAT A107 TP3 VARIES ABOVE AND BELOW GROUND. WHEN TP3 IS ABOVE GROUND, IS A107 U14 PIN 7 A TTL LOW, AND WHEN TP3 IS BELOW GROUND IS A107 U14 PIN 7 A TTL HIGH?
YES
NO
U9 OR Q8 BAD.
IS U11 PIN 6 THE SAME VOLTAGE, BUT THE OPPOSITE POLARITY, AS TP4?
YES
NO
A107 U14A BAD.
POWER METER ZERO DAC BAD.
U10 OR U11 BAD.
IS TP3 THE SAME VOLTAGE AS TP4?
YES
NO
U12 OR U13 BAD.
IS U14 PIN 1 A TTL LOW?
YES
NO
U14B BAD.
A

Figure 6-14. Power Meter and Power Meter Zero DAC

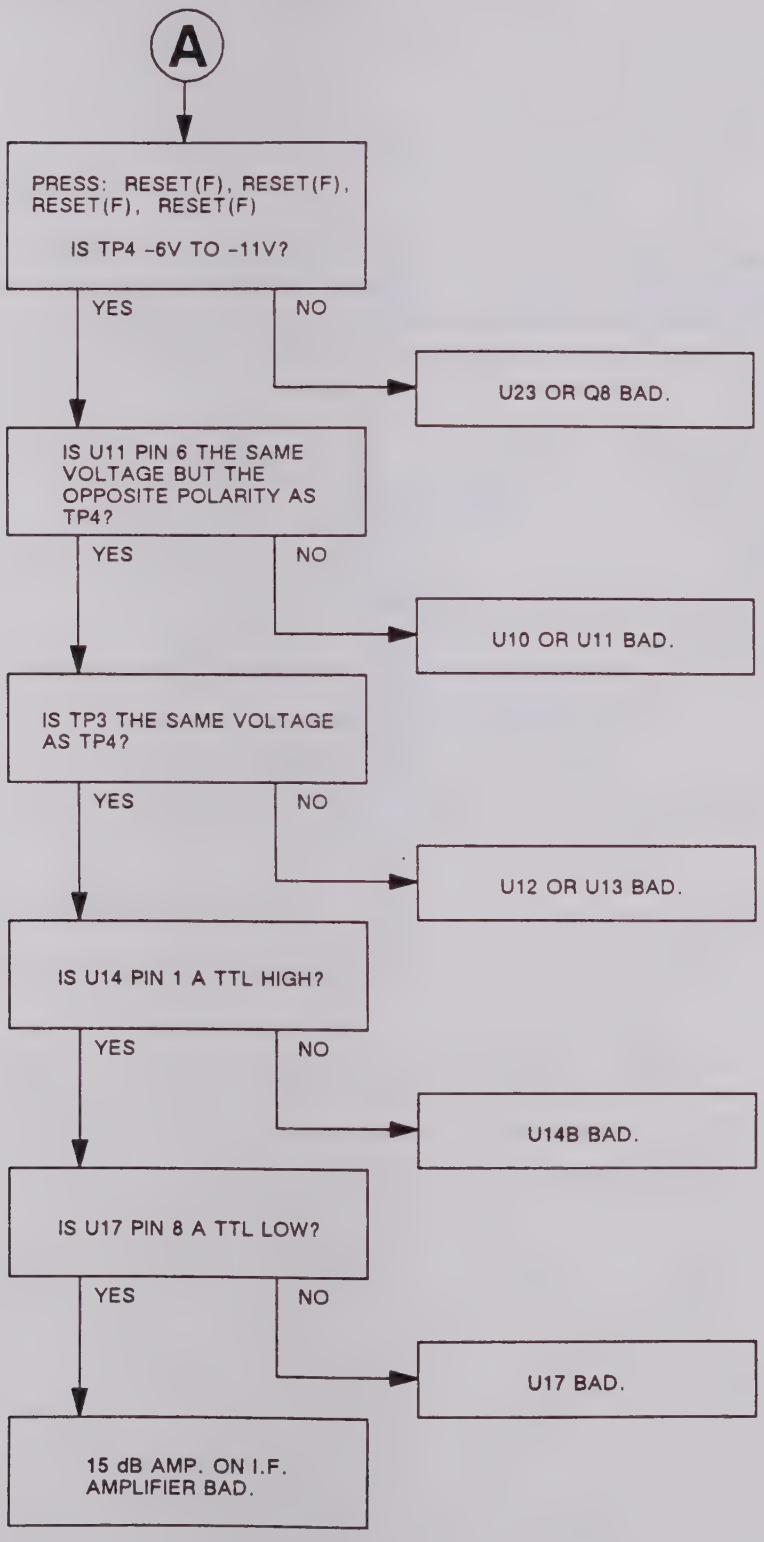


Figure 6–14. Power Meter and Power Meter Zero DAC, continued

Section 7
Adjustments and Calibrations

GENERAL

To correctly adjust the 545B or 548B counter use the following procedures. Adjustments should only be made if the counter does not operate as specified, or following the replacement of components. If the adjustments do not result in the performance specified then refer to the troubleshooting section of this manual. The test equipment required is:

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	General Purpose
Fluke	8050A	D.V.M.	4 1/4 digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
Wavetek	2002	Sweeper	10 MHz – 2 GHz
EIP	931	Microwave Source	1 GHz – 18.6 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz – 26.5 GHz
EIP	2000017	Service Kit	See Appendix A (A-3)

POWER SUPPLY ADJUSTMENTS

Prior to making any adjustments to the power supply the counter should warm up at least 20 minutes.

Voltages are measured on the back of the Power Supply board (A101).

1. Connect the Digital Volt Meter (DVM) between ground and +12V on A101, pin 1 and 8.
2. Adjust A101 R3 until the voltage measures +12.000 VCD ±.010 VDC.
3. Connect the DVM between ground and –12 V on A101, pin 1 and 18.
4. Adjust A101 R6 until the voltage measures –12.000 VDC ±.010 VDC.

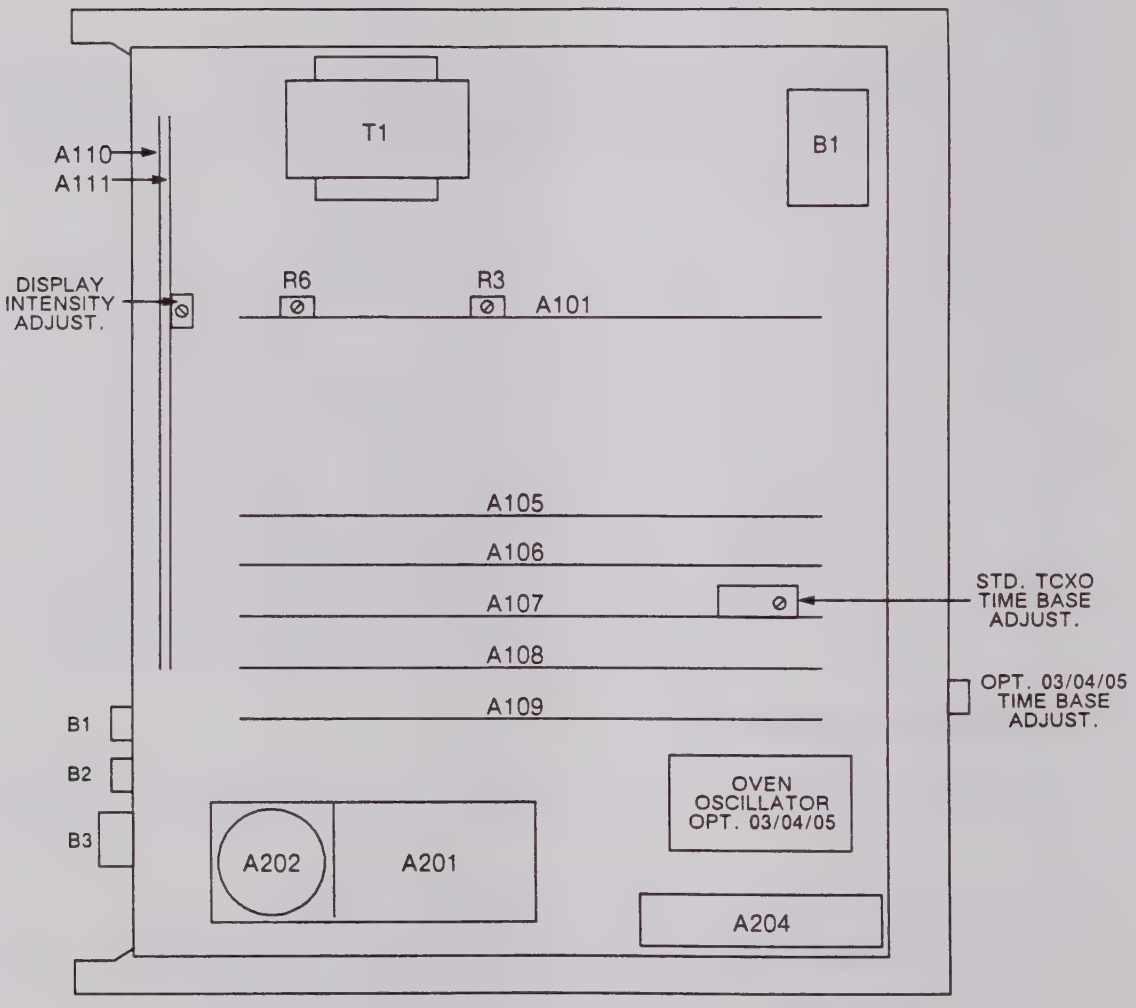


Figure 7-1. Adjustment Locations

YIG DAC CALIBRATION PROCESS

THEORY

The purpose of this process is to compensate the nonlinearity of the YIG and DAC error. The process allows a software route start in the EEPROM. The instrument generates a YIG DAC correction table, which resides in EEPROM. After the YIG searches for and centers on a signal, the software corrects the DAC reading (not the DAC itself) according to the correction table. This process yields the true YIG frequency. Then the program tunes the VCO according to the true YIG frequency instead of the ERROR DAC reading.

Each entry of the correction table contains two values:

(1) the YIG frequency and
(2) the DAC reading

Each value consists of 2 bytes. The YIG frequency is represented in hex in 2 MHz increments. For example, if the YIG frequency is 1 GHz then:

$$1\ GHz = 1000\ MHz = 2 * 500\ MHz = 2 * 01F4 \quad (hex)$$

and "01F4" is what is written to the table.

The table looks like this:

entry 1	YIG freq 1	DAC reading 1*
entry 2	YIG freq 2	DAC reading 2
. . .	. . .	. . .
. . .	. . .	. . .
entry N	YIG freq n	DAC reading n*

where N must be **at least 2 and can be as much as 248.**

* The values in entry 1 and N are extrapolated.

YIG DAC CORRECTION TABLE

Given a DAC reading D, the software first searches through the second row of the table. If D is equal to an exact DAC reading in entry n, where 1 <= m <= 248, then the software generates the corresponding YIG frequency reading. If D falls between 2 consecutive DAC readings in entry p and q, where 1 < = p < q < = 248, then the software uses a linear interpolation algorithm to find the corresponding YIG frequency Y as shown in the following equation:

If:

$$\frac{DAC\ q - DAC\ p}{YIG\ q - YIG\ p} = \frac{D - DAC\ p}{Y - YIG\ p}$$

then Y is:

$$Y = (D - DAC\ p) * \frac{YIG\ q - YIG\ p}{DAC\ q - DAC\ p} + YIG\ p$$

NOTE

When Y is being calculated, the multiplication is performed before the division to avoid precision error.

If for some reason the instrument cannot find a suitable DAC reading entry, ERROR #40 is generated to indicate error in the correction table.

CORRECTION TABLE SETUP

Setting up the correction table is actually the YIG DAC calibration process. The user enters "Test 91" to activate the process. At first the table contains two entries:

	YIG frequency	DAC number
default 1	0	0 hex
default 2	3FFF hex	3FFF hex

The user applies a synthesized signal Y1 GHz to the counter, then enters Y1 GHz through the counter's front panel or via GPIB. After the user enters the number, a routine converts that number to hexadecimal, stores it to the table as the YIG frequency of entry #2, and shifts the original entry #2 to entry #3. Then the counter sweeps the YIG to look for the signal and center the YIG on it. If the searching and centering are successful, the DAC number D1 is read and stored as DAC # of entry #2 of the table. Now the table looks like this:

default 1	0	0
entry 1	Y1	D1
default 2	3FFF	3FFF

The user can repeat the above sequence up to 246 times with the following restrictions:

(1) the sequence must be repeated at least two times.

(2) the frequency entered must be greater than the previous frequency.

If either of the two requirements above are not fulfilled or the counter cannot center the YIG on the signal, the whole process is aborted and the correction table is not altered.

After N repetitions, the correction table will be as follows:

default 1.	0	0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1.	Y N-1	D N-1
entry N.	YN	DN
default 2.	3FFF	3FFF

where 2 <= N <= 246.

Since default values are used for the first and the last entry, they must be corrected before the user exits the calibration process. The software accomplishes this task by using Y1, Y2, D1, D2 to extrapolate default 1 and Y N-1, YN, D N-1, DN to extrapolate default 2.

The equation is :

$$Y = \frac{D * (Y2 - Y1) + Y1 * D2 - Y2 * D1}{D2 - D1}$$

The final correction table looks like this:

extrapolated entry 0.	Y0	D0
entry 1.	Y1	D1
entry 2.	Y2	D2
. . .	. . .	. . .
entry N-1	Y N-1	D N-1
entry N	YN	DN
extrapolated entry N+1	Y N+1	Y N+1

where 2 <= N <= 246.

FORMAT AND ADDRESS OF THE CORRECTION TABLE

The correction table resides in EEPROM.

Address: 0C00 hex

Format:

yyyy dddd yyyy dddd .... yyyy dddd FFFF FFFF EEEE

where	"yyyy"	means 2 bytes of YIG frequency
	"dddd"	means 2 bytes of DAC reading
	"FFFF FFFF"	represents 4 bytes of end of table mark and
	"EEEE"	means for software usage.

NOTE

Before performing this procedure A108 S-1 must be open. (A108 U4 Pin 17 will be high). After calibration, S1 must be on (A108 U4 P17) low to protect calibration.

CALIBRATION PROCEDURE

MANUAL CALIBRATION

1. Press "BAND 3" on the front panel.
2. Press "TEST 91" on front panel. The counter will then display "F01".
3. Apply a synthesized 1-GHz signal at 0 dBm to Band 3 of the counter.
4. Enter "1" and press "GHz" on the front panel.
5. Counter should display "F02".
6. Apply a synthesized 1.3-GHz signal at 0 dBm to Band 3 of the counter.
7. Enter "1", ".", "3" and press "GHz" on the front panel.
8. Counter should display "F03".
9. Apply a synthesized 10-GHz signal at 0 dBm to Band 3 of the counter.
10. Enter "1", "0" and press "GHz" on the front panel.
11. Counter should display "F04".
12. Apply a synthesized 18-GHz signal at 0 dBm to Band 3 of the counter.
13. Enter "1", "8" and press "GHz" on the front panel.
14. Counter should display "F05".
15. **Go to step 28 if the model of the counter is 545B.**
16. Apply a synthesized 22-GHz signal at 0 dBm to Band 3 of the counter.
17. Enter "2", "2" and press "GHz" on the front panel.

18. Counter should display "F06".
19. Apply a synthesized 24-GHz signal at 0 dBm to Band 3 of the counter.
20. Enter "2", "4" and press "GHz" on the front panel.
21. Counter should display "F07".
22. Apply a synthesized signal 25.5 GHz at 0 dBm to Band 3 of the counter.
23. Enter "2", "5", ".", "5" and press "GHz" on the front panel.
24. Counter should display "F08".
25. Apply a synthesized signal 26.5 GHz at 0 dBm to Band 3 of the counter.
26. Enter "2", "6", ".", "5" and press "GHz" on the front panel.
27. Counter should display "F09".
28. Press "**CLEAR DATA**" to abort the process, or press "**CLEAR DISPLAY**" to exit the process.

NOTE

If the counter can not find or center on the signal, it will display an ERROR #42 message.

NOTE

The above frequencies are required to calibrate the counter. Other frequencies are at user's choice.

CALIBRATION USING GPIB CONTROLLER

1. Output "B3TA91" to the counter.
2. Command the signal source to generate 1 GHz at 0 dBm.
3. Output "1G" to the counter.
4. Command the signal source to generate 1.3 GHz at 0 dBm.
5. Output "1.3G" to the counter.
6. Command the signal source to generate 10 GHz at 0 dBm.
7. Output "10G" to the counter.
8. Command the signal source to generate 18 GHz at 0 dBm.
9. Output "18G" to the counter.
10. **Go to step 19 if the model of the counter is 545B.**
11. Command the signal source to generate 22 GHz at 0 dBm.
12. Output "22G" to the counter.

13. Command the signal source to generate 24 GHz at 0 dBm.
14. Output "24G" to the counter.
15. Command the signal source to generate 25.5 GHz at 0 dBm.
16. Output "25.5G" to the counter.
17. Command the signal source to generate 26.5 GHz at 0 dBm.
18. Output "26.5G" to the counter.
19. Output "C" to exit the calibration process or "D" to abort the process.

NOTE

When the counter has acquired the signal and is ready to accept the next frequency, the GPIB status byte bit 0 will be set to 1. This can be recognized through service request.

TIME BASE CALIBRATION

NOTE

For Option 03, 04, 05, refer to Option Section of Manual.

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = \frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)

The standard time base oscillator used in the counter is a TCXO (A113). The range of the actual measured frequencies of the oscillator will differ by no more than 1 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate in proportion to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C), the slope of the frequency vs. temperature curve is normally no worse than $\pm 1 \times 10^{-7}$ parts per degree C. When the counter

is used in an ordinary laboratory environment, the TCXO may be set as close to 10,000,000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5° C will result in a measured signal error of no more than $\pm 2.5 \times 10^{-7}$ parts. This signal error is due to the temperature characteristics of the Time Base Oscillator.

The natural aging characteristics of the crystal in the Time Base Oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is as specified. This may improve when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operation temperature range one month after proper initial adjustments, the inaccuracy could vary from $+1.3 \times 10^{-6}$ parts to -0.7×10^{-6} parts.

TCXO CALIBRATION PROCEDURES

METHOD 1 (with accurate frequency counter)

1. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

2. Measure the frequency of the TCXO (at the rear panel 10 MHz connector) with a second counter of known calibration accuracy.

3. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

METHOD 2 (with accurate frequency source)

1. Apply a 10 000 000 Hz signal from a frequency standard (or other oscillator of suitable accuracy and stability) to the Band 1 input of the counter.

2. Press RESOL [ ] [0] (1 Hz resolution)

3. Adjust the TCXO until the reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example, if the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the counter displays 9 999 997 Hz.

DISPLAY INTENSITY

On the front panel logic assembly (A111), R4 may be adjusted to provide the most comfortable display intensity.

Section 8
Performance Tests

GENERAL

These tests are for the basic counter. Performance tests for options are in Section 10. These tests will enable the user to verify that the counter is operating within specifications.

VARIABLE LINE VOLTAGE

During the performance tests, the counter should be connected to the power source, through a variable voltage device, so that line voltage may be varied ±10% from nominal. This will assure proper operating of the counter under various supply conditions.

REQUIRED TEST EQUIPMENT (or equivalent)

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
EIP	931	Microwave Source	1 GHz - 18.6 GHz
H.P.	8350, 83570A	Microwave Sweeper	18 GHz - 26.5 GHz

BAND 1 (10 Hz - 100 MHz)

1. Set the counter to Band 1.
2. Connect the signal source output, through a 50 ohm shunt feedthrough resistor, to the Band 1 input on the counter.
3. Set the signal level to 25 mv RMS (-19 dBm into 50 ohms).
4. Vary the signal from 10 Hz to 100 MHz (changing signal source as required).

The counter should display the correct input frequency.

BAND 2
(10 MHz – 1 GHz)

1. Set the counter to Band 2.
2. Connect the signal source output to the Band 2 input of the counter.
3. Set the signal level to –20 dBm (22 mv RMS).
4. Vary the signal input from 10 MHz to 1 GHz.

The counter should display the correct input frequency.

BAND 3
(548B: 1 GHz – 26.5 GHz)
(545B: 1 GHz – 20 GHz)

1. Set the counter to Band 3.
2. Connect the signal source output to the Band 3 input of the counter.
3. Vary the signal frequency from 1 GHz to 20/26.5 GHz (changing the signal source as required) at the following levels.

1 GHz – 12.4 GHz	–30 dBm (7 mv RMS)
12.4 GHz – 20 GHz	–25 dBm (12 mv RMS)
20 GHz – 26.5 GHz	–20 dBm (22 mv RMS)

The counter should display the correct input frequency.

Section 9
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration of componant location, and a schematic diagram for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSEMBLY.

REFERENCE DESIGNATORS

A	Assembly	J	Jack or Connector	S	Switch
B	Battery or Fan	K	Relay	T	Transformer
C	Capacitor	L	Inductor	TP	Test Point
CR	Diode	P	Plug or PCB Contacts	U	Integrated Circuit
DS	Indicator (Display)	Q	Transistor	X	Socket or Holder
F	Fuse	R	Resistor		

ABBREVIATIONS

CBN	Carbon	MTCH PR	Matched Pair
CER	Ceramic	NOM	Nominal
CMT	Cermet	PC	Printed Circuit
CNTR	Counter	PCB	Printed Circuit Board
CONV	Converter	pF	Picofarad
COMP	Composition	PREC	Precision
CONN	Connector	PROM	Programmable Read Only Memory
ELEC	Electrolytic	RAM	Random Access Memory
FDTH	Feedthrough	RSTR	Resistor
FLM	Film	RT AN	Right Angle
FML	Female	S.A.T.	Value or type selected at factory test. Part may not be used.
GP	General Purpose		
IC	Integrated Circuit	SW	Switch
K	Kilo (x 1,000)	TANT	Tantalum
LED	Light Emitting Diode	TRIM	Trimmer
M	Mega(a) (x 1,000,000)	µF	Microfarad
MET OX	Metal Oxide	µH	Microhenry
MF	Metal Film	VAR	Variable
mH	Millihenry	WPRF	Waterproof
ML	Male	WW	Wirewound
		XSTR	Transistor

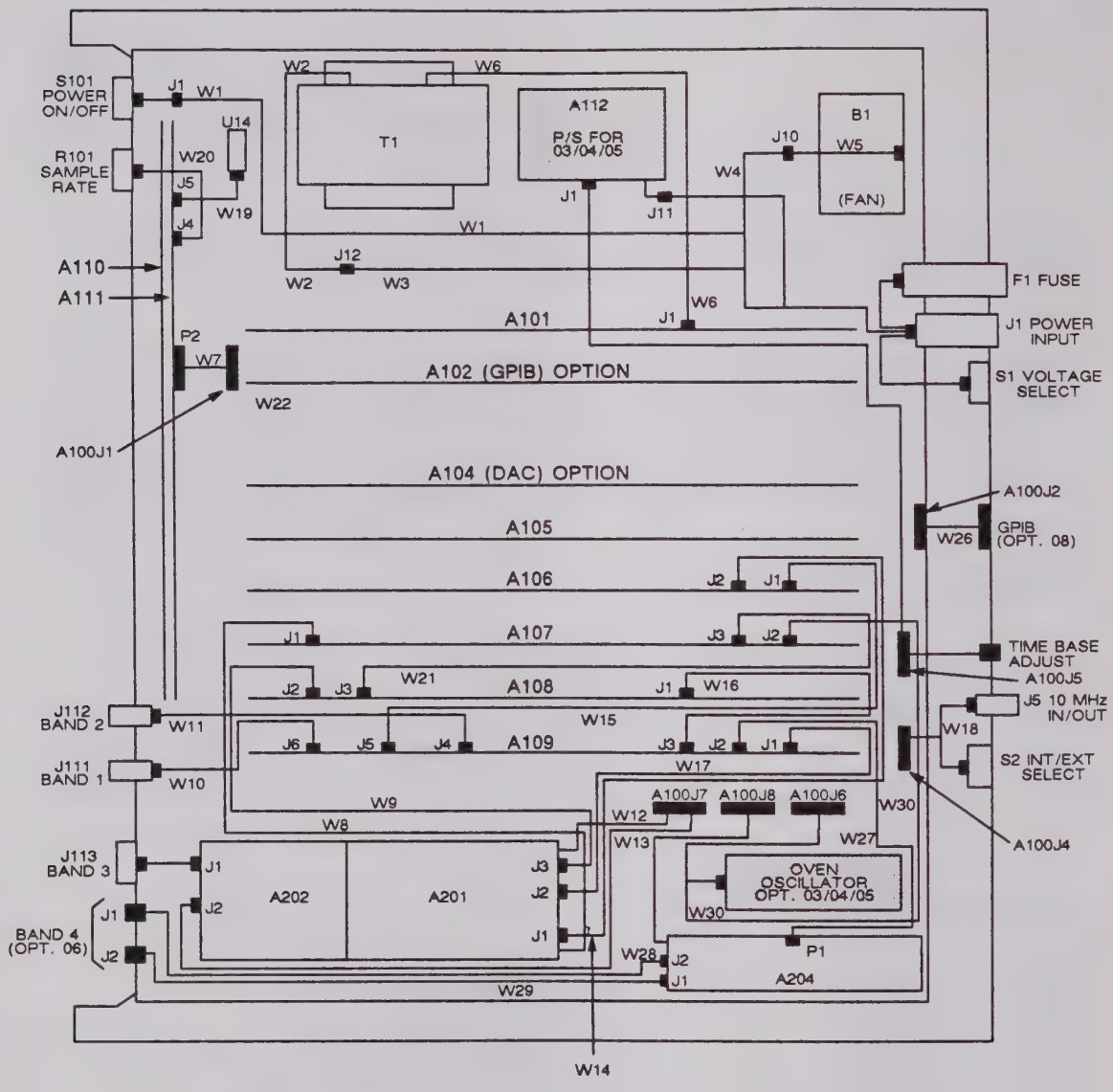


Figure 9-1. Assembly Locations and Cable Connections in Counter

CABLE CONNECTION GUIDE

FROM	CABLE	TO
A1S101J1	W1	A1S1,F1,J1
A1J12	W2	A1T1
A1S1	W3	A1J12
A1J10	W4	A1S1
A1B1	W5	A1J10
A101J1	W6	A1T1
A111P2	W7	A100J1
A107J1	W8	A201
A108J2	W9	A201J3
A1J111	W10	A109J6
A1J112	W11	A109J4
A201	W12	A100J7
A202J2	W13	A100J7
A106J2	W14	A201J1
A106J1	W15	A109J5
A108J1	W16	A109J3
A109J1	W17	A201J2
A1J5,S2	W18	A100J4
A1U14	W19	A111J5
A1R101	W20	A111J4
A107J3	W21	A108J3
A100J2	W26	A1,GPIB (OPT 06)
A204P1	W27	A109J2 (BAND 4, OPT 06)
A204J2	W28	A1J1 (BAND 4, OPT 06)
A204J1	W29	A1J2 (BAND 4, OPT 06)
A107J2	W30	A100J6 (OPT 03/04/05)

545B/548B MICROWAVE FREQUENCY COUNTERS

(545B) 2000022-13
(548B) 2000023-13

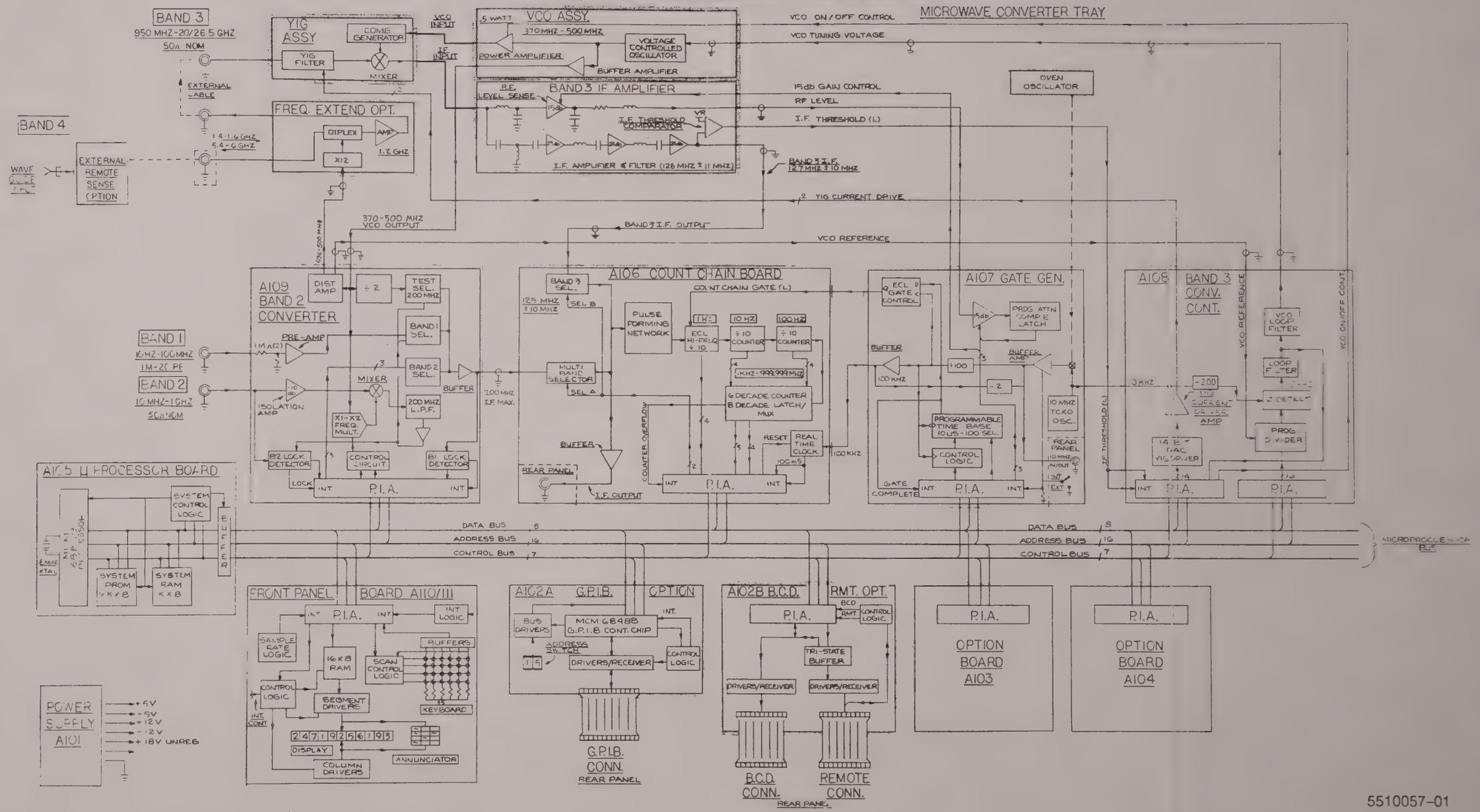
REF DES.	DESCRIPTION	EIP NO.	UNITS PER ASSY
	PANEL ASSY,FRONT,545B	2101802-01	1
	PANEL ASSY,FRONT,548B	2010802-02	1
	OVERLAY,FRONT PANEL,545B	5210373-05	1
	OVERLAY,FRONT PANEL,548B	5210374-05	1
	SAMPLE RATE ASSY,545	2010134-01	1
	SWITCH ASSY,POWER,58X	2010187-02	1
	KNOB,MOD 5XX	5210223-00	1
	BUTTON,SET (MF 5230005-02)	5210220-00	1
	PIN,ALIGNMENT,545 DISPLAY	5210190-00	2
	RETAINER,KEY,545	5210191-00	1
	PANEL,FRONT,FLAT,5XX	5210378-01	1
	PANEL ASSY,REAR,5XX	2010219-01	1
	PANEL,REAR,FINISH,54X	5210379-00	1
	CONN,JACK/TAB BNC BHD (TR5 FNSH)	2610024-00	1
	CONN,RCPT,PWR,W/FILTER	2650005-00	1
	SWITCH,TGL, SPDT 120V 5A	4510001-00	1
	SWITCH ASSY,VOLT SELECT,545	2010159-01	1
	CARRIER,FUSE,3AG,GREY(DOM)	5000171-00	1
	HOLDER,FUSE,W/MTG NUT	5000170-00	1
	FUSE,1AMP SB 3AG 250V	5000085-00	1
	FAN ASSY	2010136-02	1
	FAN,115 VOLT AC	5000151-00	1
	CONN,PLUG,MINTR,3 PIN,W/O	2620110-00	1
	CONN,CONTACT,MALE	2620038-00	2
	SPACER,FAN MTG	5210404-00	2
	FRAME SET ASSY,14IN.	2010151-02	1
	PANEL,SIDE,5XX	5210312-00	2
	TRIM STRIP,FRONT POST	5220004-00	2
	STRIP,HANDLE,FOR 5250011	5220025-00	2
	FRAME,MOD,14IN (MF 5240001-14)	5210248-00	2
	CORNER POST,FRONT,MACHINED	5210311-00	2
	EXTRUSION,CORNER POST,REAR	5250002-00	2
	HANDLE,ENCLOSURE (MF 5250011-01)	5250011-00	2
	XFMR ASSY,PWR,5XX	2010359-01	1
	XFMR,PWR,5XX	4900011-00	1
	CONN,PLUG,MINTR,9 PIN,W/O	2620112-00	1
	CONN,CONTACT,MALE	2620038-00	7
	CONN,CONTACT,FEM	2620036-00	1
	CARD GUIDE, FRONT,TYPE 2, UNIVERSAL	5210804-01	1
	CARD GUIDE, REAR,TYPE 2, UNIVERSAL	5210805-01	1
	COVER ASSY,TOP,54X/57X	2010212-01	1
	COVER,ENCL BOTTOM,14IN	5210209-00	1
	BAIL,TILT	5000055-00	1
	FOOT,MOLDED,BLK	5220003-00	4
	CORD,LINE 3-COND	5440002-00	1

545B/548B MICROWAVE FREQUENCY COUNTERS (Continued)

(545B) 2000022-13
(548B) 2000023-13

REF DES.	DESCRIPTION	EIP NO.	UNITS PER ASSY
	PCB ASSEMBLIES		
A100	COUNTER INTERCONNECT	2020180-01	1
A101	POWER SUPPLY	2020222-06	1
A105	MICROPROCESSOR	2020215-02	1
A106	COUNT CHAIN	2020136-03	1
A107	GATE GENERATOR	2020197-09	1
A108	CONVERTER CONTROL	2020200-07	1
A109	BAND 2 CONVERTER	2020139-07	1
A110	FRONT PANEL DISPLAY AND KEYBOARD	2020140-02	1
A111	FRONT PANEL LOGIC	2020191-02	1
A203	BAND 3 MICROWAVE CONVERTER, 535B	2010241-08	1
	BAND 3 MICROWAVE CONVERTER, 538B	2010241-07	1
	CABLES		
W7	FLAT RBN,F/P LOGIC	2040169-01	1
W9	SRC ASSY,545 (VOLT TUNE)	2040174-01	1
W10	COAX ASSY,B1,545	2040165-01	1
W11	COAX ASSY,B2,545	2040166-01	1
W14	COAX ASSY,IF OUT,545	2040172-01	1
W15	COAX ASSY,LO BAND,545	2010210-01	1
W16	COAX ASSY,VCO RF,545	2040208-01	1
W17	COAX ASSY,RF OUT,545	2040175-01	1
W18	HARN ASSY,PANEL,REAR,545	2040167-01	1
W19	HARN ASSY,REG,F/P	2040168-01	1
W21	HARN ASSY,GG,54XA	2040227-01	1
	PROMS		
A105	PROM SET,BASIC,545B/548B	2060035-01	1
U11	PROM,PROG,GPIB OPT,545B/548B	6500035-01	1
U12	PROM,PRGM,BASIC 2,545B/548B	6500035-02	1
U13	PROM,PRGM,BASIC 3,545B/548B	6500035-03	1

NOTE: REVISION LEVEL OF PROMS MUST BE SPECIFIED WHEN ORDERING PROM SET.



5510057-01

Figure 9-2. 545B/548B Block Diagram

A100
COUNTER INTERCONNECT
(2020180-01)

FUNCTIONAL DESCRIPTION
NOT REQUIRED

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A100 COUNTER INTERCONNECT ASSY 2020180-01

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
J1		CONN,PCB HEADER,26 PIN,W/EJCTR	2620078-00	1
J2		CONN,PCB,HEADER,50 PIN,W/EJCTR	2620081-00	2
J3	J2			
J4		CONN,PCB,FRICT LK 156,4 PIN	2620061-00	1
J5		CONN,FRICT LK 156,6 PIN	2620090-00	1
J6		CONN,HEADER,STR .156,7 PIN	2620186-00	1
J7		CONN,HEADER,STR .156,10 PIN	2620187-00	1
J8		CONN,FRICT LK .100,4 PIN	2620068-00	1
XA101		CONN,PCB EDGE,AMPL,11 PIN	2620183-00	1
XA102		CONN,PCB EDGE,50 PIN	2620185-00	1
XA103		CONN,PCB EDGE,30 PIN	2620184-00	7
XA104	XA103			
XA105	XA103			
XA106	XA103			
XA107	XA103			
XA108	XA103			
XA109	XA103			

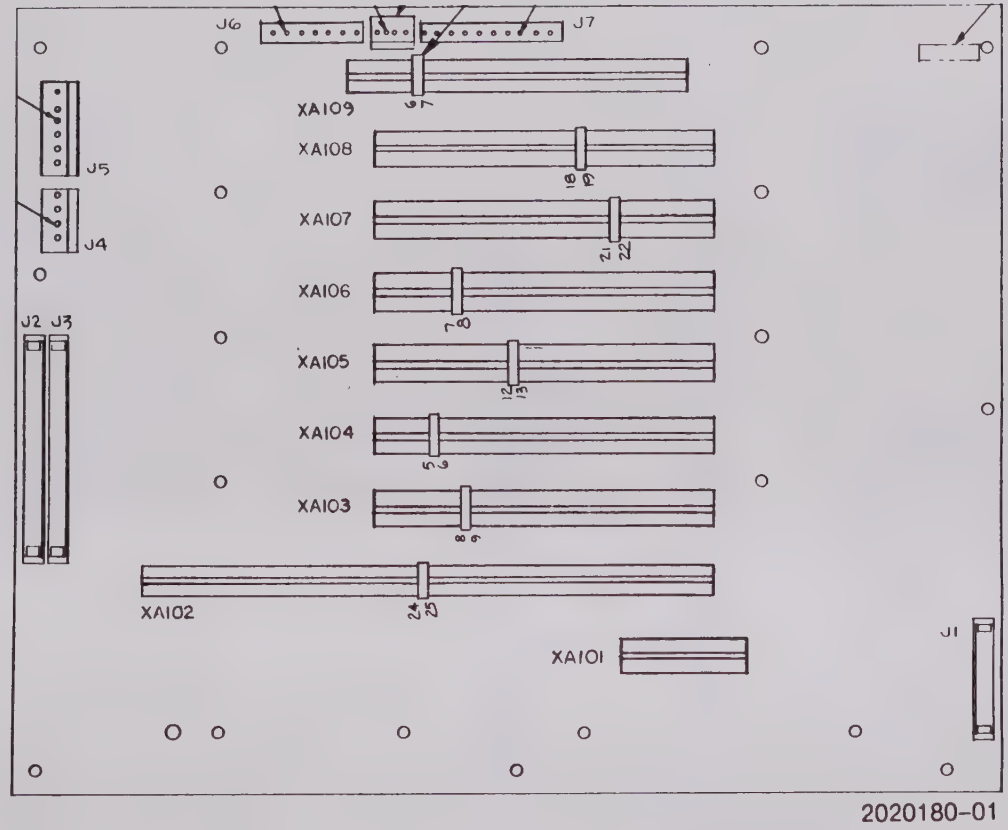
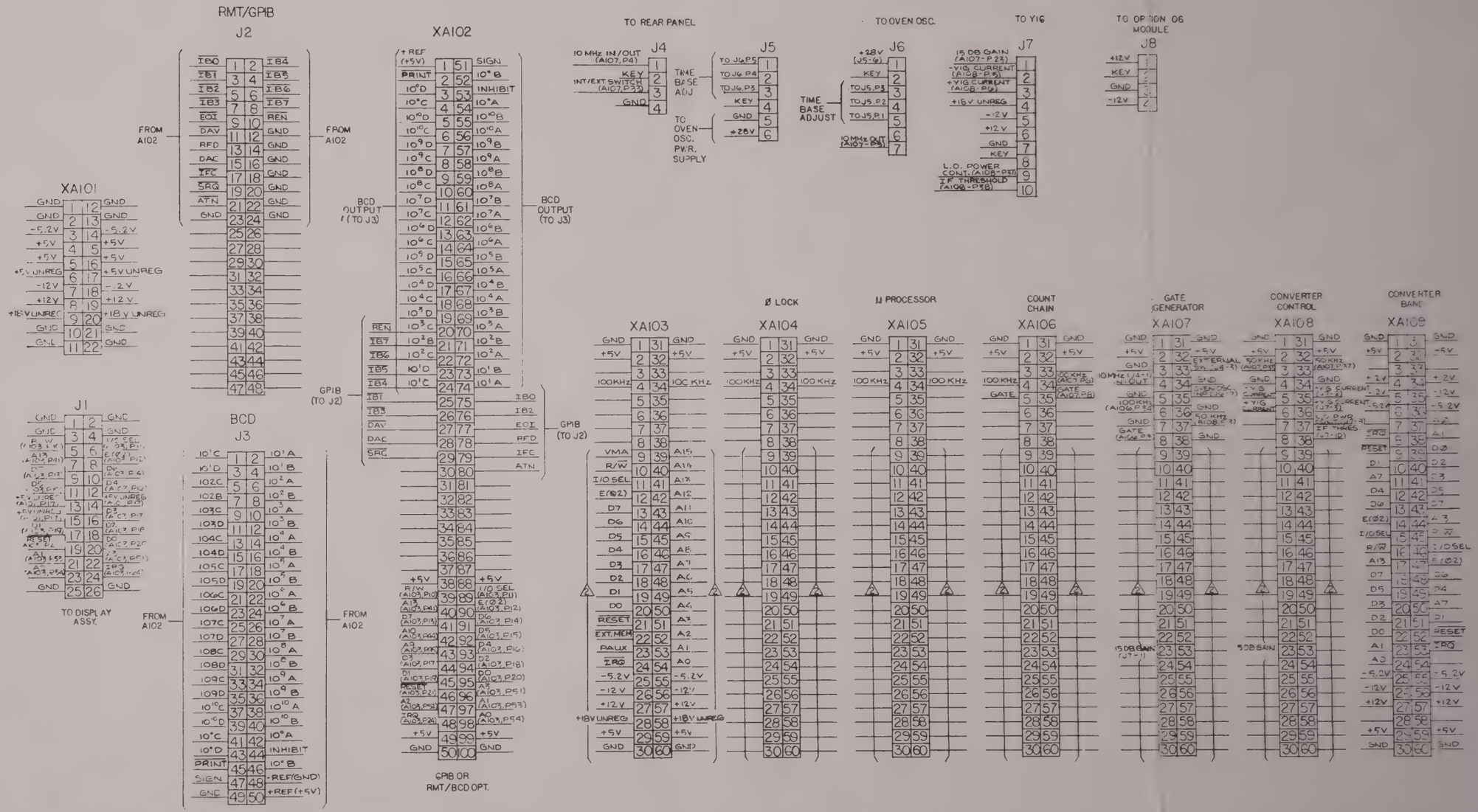


Figure 9-3. Component Locator, Counter Interconnect



△ XA103 THRU XA106 HAVE COMMON CONNECTIONS ON LINES SHOWN IN BRACKETS.

5500180-00

Figure 9-4. Schematic Diagram, Counter Interconnect

A101
POWER SUPPLY
(2020222-06)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies.

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1), primary wiring, F1 fuse (100/120V), the 220/240V power programming switch, and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, -5.2V, +12V and -12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of ±9V and ±18V.

The unregulated +18V is used directly as one supply voltage for the microwave converter. The +18V is also regulated to +12V by a LM317 three-terminal series regulator employing thermal current protection. The -18V is regulated to -12V by a LM337 three-terminal series regulator also employing thermal current protection.

The unregulated +9V is regulated to +5V and is used to drive the front panel. The +9V and -9V unregulated supplies are also used for the +5V and -5.2V supplies and are each regulated by a single three-terminal regulator that contains internal thermal and current shutdown circuitry.

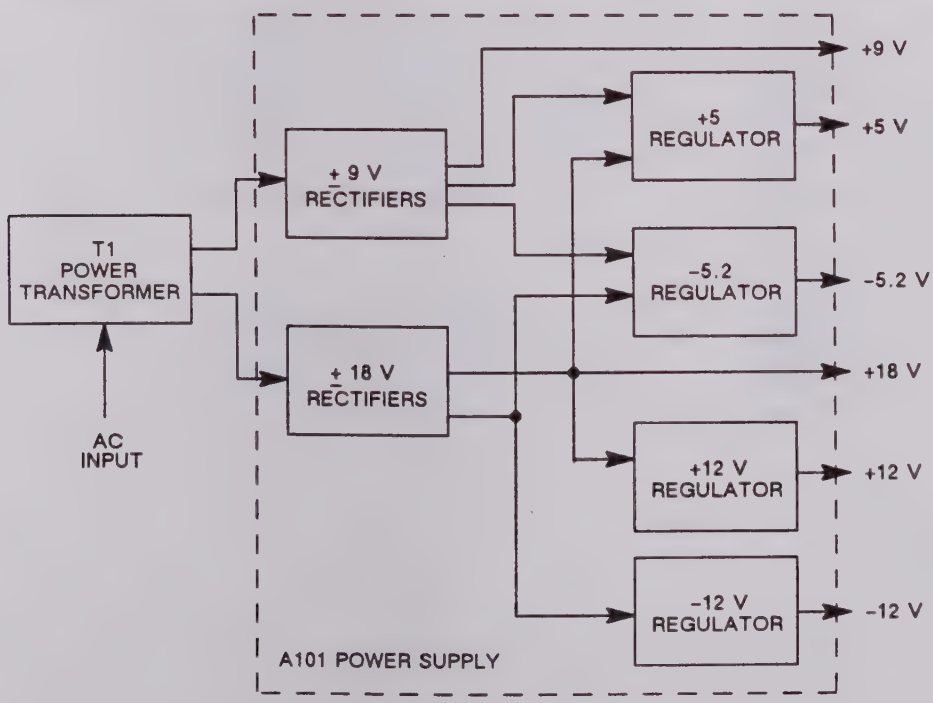


Figure 9-5. Power Supply Functional Diagram

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A101 POWER SUPPLY ASSEMBLY 2020222-06

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ELCTLT	32000µF	20%	15V	2200019-00	1
C2		CAP,ELCTLT	27000µF		15V	2200027-00	1
C3		CAP,TANTALUM	10µF	20%	25V	2300029-00	4
C4		CAP,ELCTLT	14000µF		25V	2200017-00	1
C5		CAP,ELCTLT	9500µF	20%	25V	2200016-00	1
C6	C3						
C7		CAP,TANTALUM	1µF		35V	2300008-00	3
C8	C3						
C9		CAP,TANTALUM	22µF		35V	2300034-00	1
C10	C3						
C11	C7						
C12	C7						
C13		CAP,ML CER	1µF	20%	50V	2150023-00	4
C14	C13						
C15	C13						
C16	C13						
CR1		DIODE,MDA970-2,BRIDGE,100V				2710045-00	1
CR2		DIODE,MDA990-1,BRIDGE				2710028-00	1
J1		CONN,SQ POST,6 PIN,156				2620157-00	1
J2		CONN,POST,SQ 156,3 PIN				2620154-00	1
R1		RES,MF	475	1/10W	1%	4504750-00	1
R2		RES,MF	3.01K	1/8W	1%	4053011-00	1
R3		POT,CERMET	2.0	KT05	0.5W	4250016-00	2
R4		RES,CC	5.1	1W	5%	4030519-00	2
R5	R4						
R6	R3						
R7		RES,MF	8.66K	1/8W	1%	4068661-00	1
R8		RES,MF	1.21K	1/10W	1%	4051211-00	1
R9		RES,M/OX	200	1/4W	2%	4130201-00	1
R10		RES,CC	5.6	1/4W	5%	4010569-00	1
R11		RES,M/OX	13	1/4W	2%	4130130-00	1
R12		RES,CC	4.7	1/4W	5%	4010479-00	1
TP1		CONN,PIN-TP,SWAGE .040D-.150L				2620193-00	4
TP2	TP1						
TP3	TP1						
TP4	TP1						
U1		IC,78H05A,VOLT RGLTR,+5V,TO-3				3057805-01	1
U2		IC,LM317,VOLT RGLTR,ADJ,POS,TO-220				3040317-00	1
U3		IC,LM337,VOLT RGLTR,ADJ,NEG,TO-220				3040337-00	1
U4		IC,LM345-5.2,VOLT RGLTR,NEG,TO-3				3040345-00	1

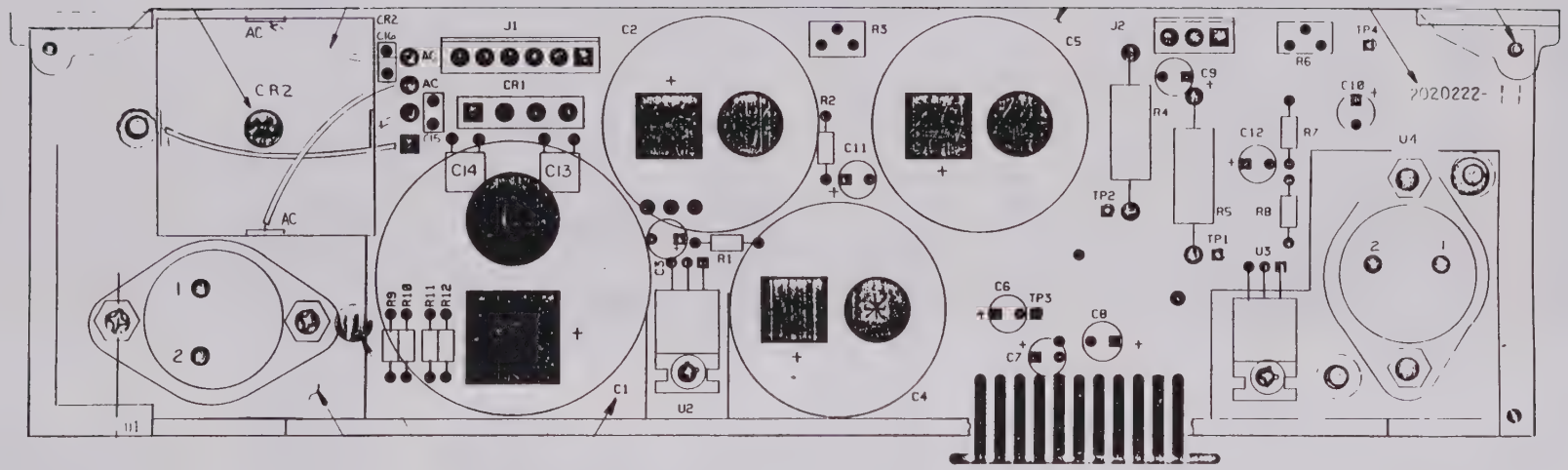
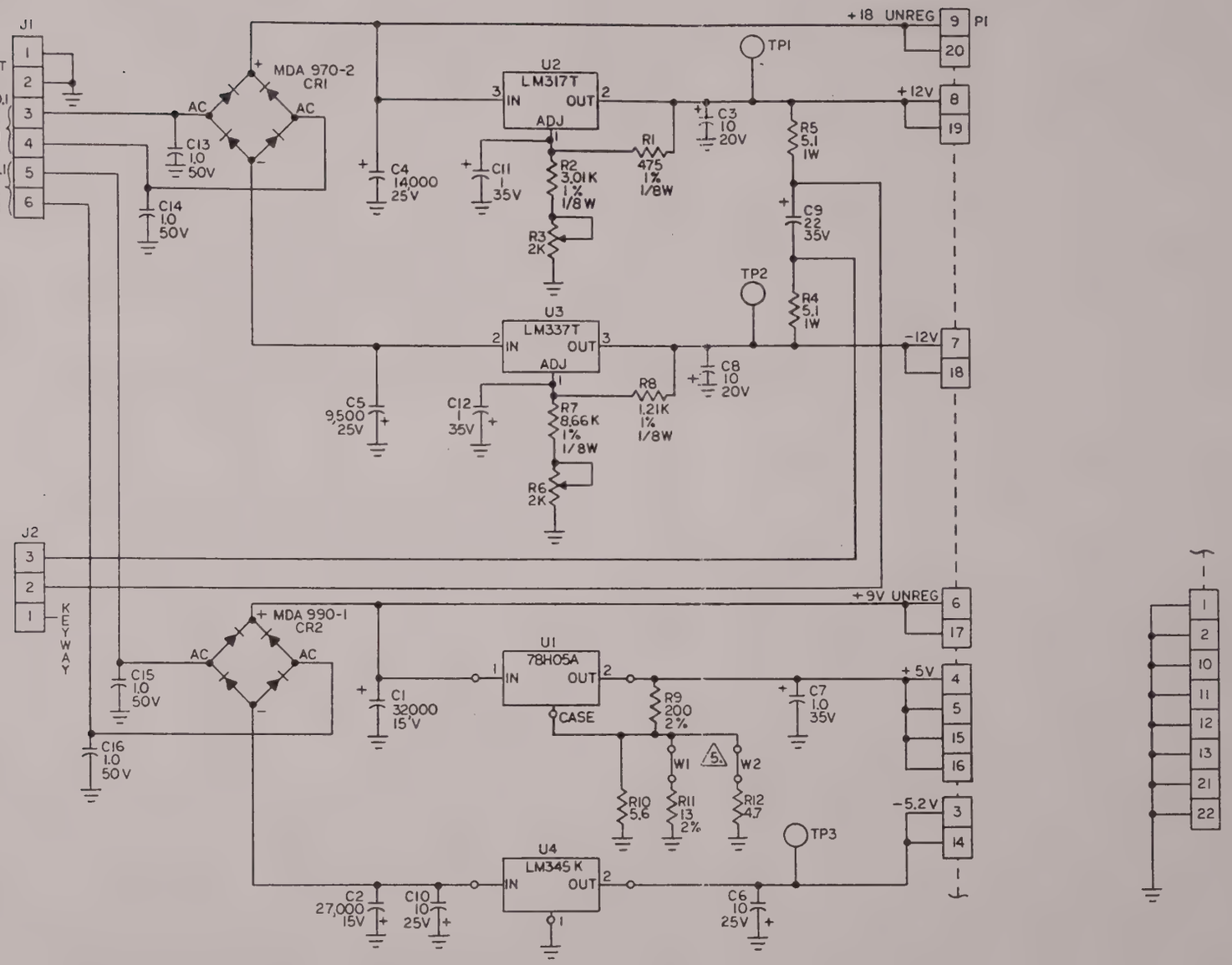


Figure 9-6. Component Locator, Power Supply



5500222-02

Figure 9-7. Schematic Diagram, Power Supply

A105
MICROPROCESSOR
(2020215-02)

The Microprocessor Board contains the microprocessor, the control logic, and the firmware for controlling the operation of the counter. The board can be divided into five functional blocks.

1. Microprocessor
2. Power-up Reset Circuit
3. Address Decoder
4. RAM and Program Memory
5. Control Logic and Buffers

MICROPROCESSOR

The counter uses a Motorola 68B09 microprocessor. The clock generation circuitry for the digital system is contained within the 68B09. The only external components required for clock generation are two 24-pF capacitor and an AT-cut 8-MHz crystal.

The NMI, FIRO, and DMA functions of the 68B09 are not used. Their corresponding control lines are always disabled. The processor state indicators (BS, BA) are also not used by the counter. The HALT and the MRDY controls are connected to the Interconnect board through the edge connector.

POWER-UP RESET CIRCUIT

The Power-up Reset circuit provides a 100-ms reset signal to the entire digital system after the counter is turned on. The reset signal remains true as long as the +5-volt power supply stays below +4 volts.

When the counter is turned on, the voltage across C5 is 0 volts. The output of the comparator U1 is at logic low. The capacitor C5 slowly charges up through R2. The output of the comparator remains low as long as the voltage across C5 is lower than the voltage on pin 3 of the comparator. When the voltage across C5 becomes higher than that on pin 3, the output of the comparator becomes true, removing the reset signal. R3 is provided for hysteresis purposes. When power is removed, C5 will discharge quickly through CR1.

ADDRESS DECODER

The address decoding is performed by a 4-to-16 line decoder. The 64K-byte address space is divided into sixteen 4K-byte blocks, one of which is always enabled.

The enable signals for the memory blocks become true no later than 51 ns after Q. They stay true until a maximum of 40 ns after E has become false. The 4-to-16-line decoder has open collector outputs. This enables the addressed memory block to be enlarged by wire-ORing two or more outputs together.

The memory map for the counter is as follows:

Volatile RAM Memory	0000 – 07FF
Non-Volatile RAM Memory	0800 – 0FFF
I/O	1000 – 2FFF
Signature Analysis	3000 – 3FFF
Program Memory	4000 – FFEF
Reserved (68B09)	FFF0 – FFF1
	FFF2 – FFF3
	FFF4 – FFF5
	FFF6 – FFF7
IRQ	FFF8 – FFF9
	FFFA – FFFB
	FFFC – FFFD
RESET	FFFE – FFFF

RAM AND PROGRAM MEMORY

RAM

A 2K-byte-wide volatile RAM is provided for the normal operation of the counter. To prevent data from being erroneously written into the RAM, the chip enable signal is active only when the E clock and the RAM memory block enable signal from the address decoder are both active and when the A11 address line is at logic 1.

PROM

A block of 48K bytes of memory are assigned for system program. The Microprocessor board contains three 28-pin sockets for PROMs. Each of the sockets is wired to accept a 16K-byte PROM.

CONTROL LOGIC AND BUFFERS

The digital system of the counter contains three buses: the data bus, the address bus, and the control bus.

DATA BUS

The data bus originates from the microprocessor. For signature analysis, the data bus can be disconnected from the rest of the system at the microprocessor by removing jumper header E1. The data bus on the microprocessor board is buffered from the rest of the digital system. The data bus buffer is enabled only when the address space assigned to I/O is addressed. The direction of the data bus buffer is determined by the state of the R/W control line.

ADDRESS BUS

The address bus also originates from the microprocessor. The address bus buffer is always enabled.

CONTROL BUS

The control bus contains eight control lines. Five of the control lines originate from the Microprocessor board. The other three control lines originate from the rest of the digital system.

R/W, E, and Q originate from the microprocessor. Reset is supplied by the power-up reset circuit. The I/O SEL control line is true when A15 and A14 are at logic 0 and either A13 or A12 or both are at logic 1 levels. The IRQ control line is the wired-OR of the interrupt request lines. MRDY is the wired-OR of the memory ready control lines. The MRDY and HALT control lines are provided for future expansion.

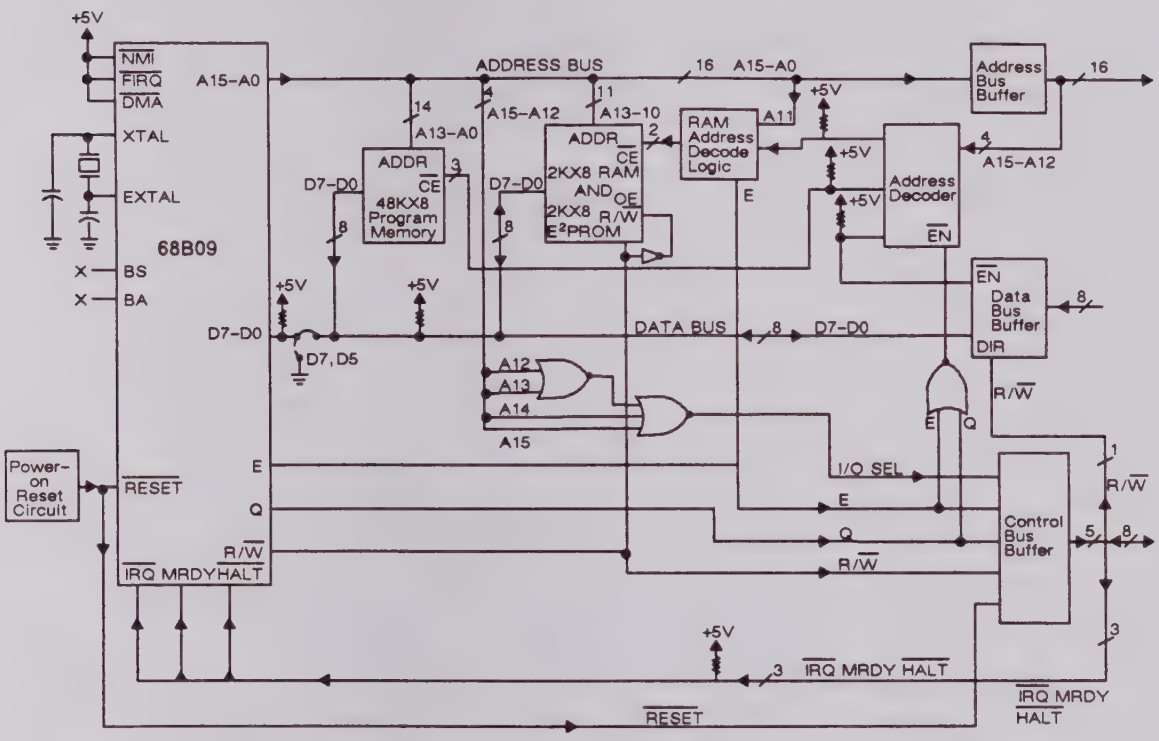


Figure 9-8. Functional Block Diagram, Microprocessor

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A105 MICROPROCESSOR 2020215-02

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,MICA	18PF	5%	500V	2260015-00	2
C2	C1						
C3		CAP,CER	.01µF	20%	100V	2150003-00	14
C4	C3						
C5		CAP,TANTALUM	3.9µF	10%	15V	2300027-00	1
C6	C3						
C7	C3						
C8	C3						
C9		CAP,TANTALUM	33µF		10V	2300015-00	2
C10	C3						
C11	C3						
C12	C3						
C13	C3						
C14	C3						
C15	C3						
C16	C3						
C17	C3						
C18	C3						
C19	C9						
C20		CAP,ML CER	.001µF	10%	100V	2150015-00	1
CR1		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
CR2		DIODE,1N5228,ZENER 3.9V				2705228-00	1
E1		HEADER,PROGRAM DIP 16 PIN				5000205-00	1
R1		RES,CC	1M	1/4W	5%	4010105-00	1
R2		RES,CC	22K	1/4W	5%	4010223-00	1
R3		RES,CC	300K	1/4W	5%	4010304-00	1
R4		NOT USED					
R5		RES,CC	240	1/4W	5%	4010241-00	1
R6		RES,CC	4.7K	1/4W	5%	4010472-00	4
R7	R6						
R8	R6						
R9	R6						
RN1		RES,NTWK	9X10K	0.2W	2%	4170003-00	3
RN2	RN1						
RN3	RN1						
RN4		RES,NTWK,SIP	9X4.7K		2%	4170014-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	10
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
TP6	TP1						
TP7	TP1						
TP8	TP1						
TP9	TP1						
TP10	TP1						
U1		IC,LM311,VOLT COMPARATOR				3050311-00	1
U2		IC,68B09,MP,8-BIT,2MHZ				3050025-00	1
U3		IC,74LS365				3084365-00	1
U4		NOT USED					
U5		IC,74LS27				3087427-00	1
U6		IC,74LS244				3084244-00	2
U7		NOT USED					
U8		IC,74LS245				3084245-00	1
U9		IC,6116,2KX8 BIT RAM,CMOS				3056116-00	1

A105 MICROPROCESSOR (Continued) 2020215-02

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
U10		PROM,2KX8	6420000-00	1
U11		PROM,PRGM,BASIC 1,545B/548B	6500035-01	1
U12		PROM,PRGM,BASIC 2,545B/548B	6500035-02	1
U13		PROM,PRGM,BASIC 3,545B/548B	6500035-03	1
U14		IC,74LS10	3087410-00	1
U15	U6			
U16		IC,74159	3074159-00	1
U17		IC,74LS04	3087404-00	1
XU1		CONN,SOCKET,DIP,8 PIN	2630014-00	1
XU2		CONN,SOCKET,DIP,40 PIN	2630022-00	1
XU3		CONN,SOCKET,DIP,16 PIN	2630016-00	3
XU4		NOT USED		
XU5		CONN,SOCKET,DIP,14 PIN	2630015-00	3
XU6		CONN,SOCKET,DIP,20 PIN	2630018-00	3
XU7		NOT USED		
XU8	XU6			
XU9		CONN,SOCKET,DIP,24 PIN	2630020-00	3
XU10	XU9			
XU11		CONN,SOCKET,DIP,28 PIN	2630021-00	3
XU12	XU11			
XU13	XU11			
XU14	XU5			
XU15	XU6			
XU16	XU9			
XU17	XU5			
XE1	XU3			
XE2	XU3			
Y1		CRYSTAL,8.000MHZ (MP808A)	2030010-00	1

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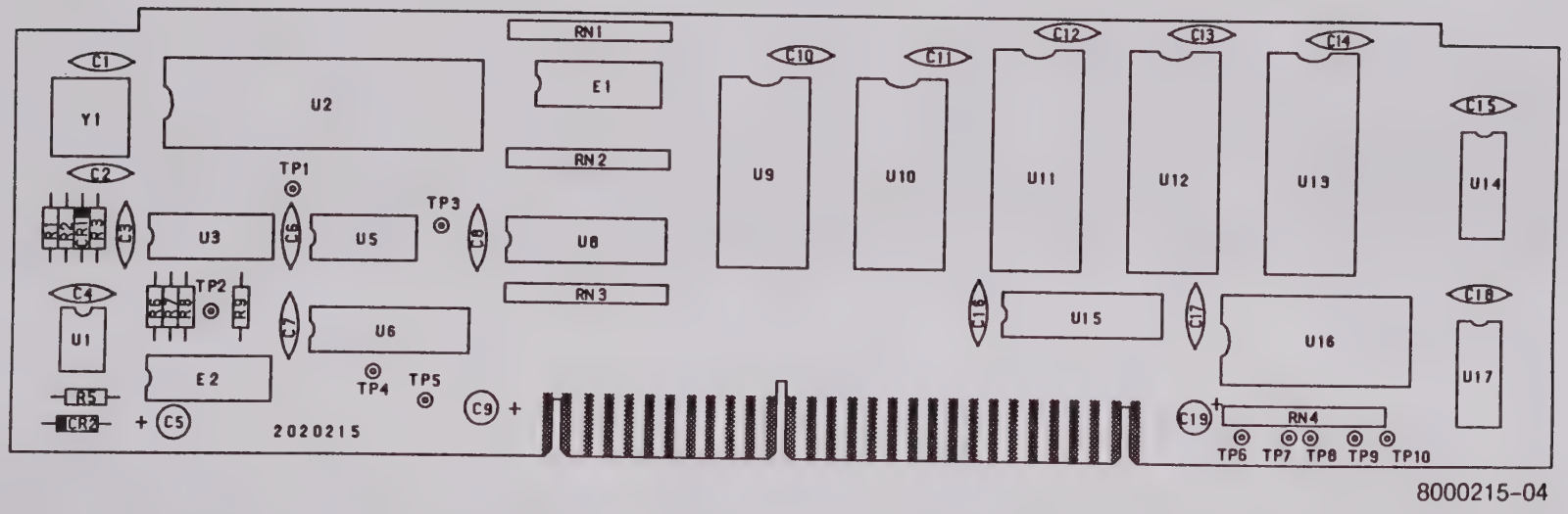
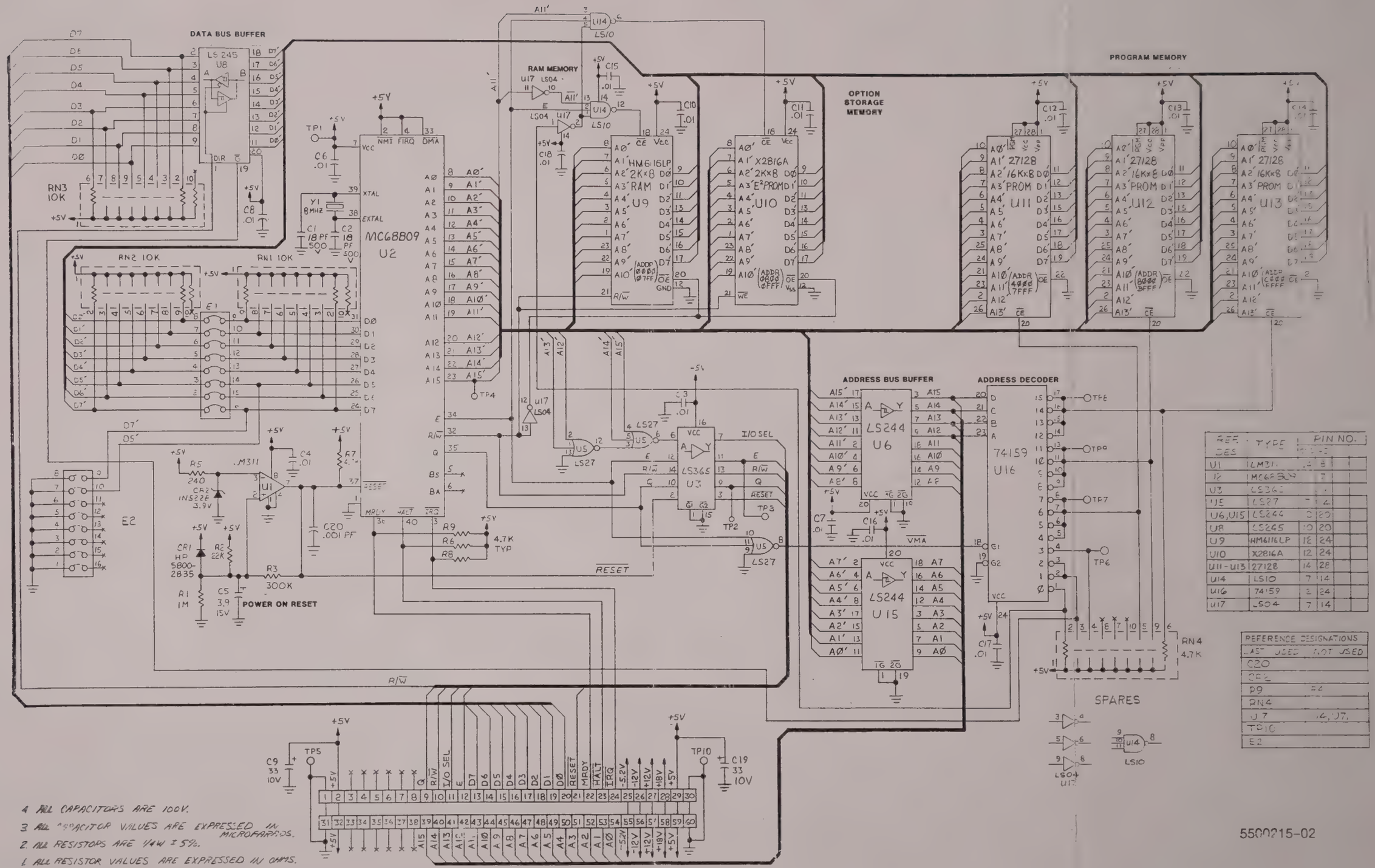


8000215-04

Figure 9-9. Component Locator, Microprocessor



REF DES	TYPE	PIN NO.	
U1	LM311	4	8
U2	MC6B09	1	7
U3	LS365	8	16
U5	LS27	7	14
U6,U15	LS244	10	20
U8	LS245	10	20
U9	HM6116LP	12	24
U10	X2816A	12	24
U11-U13	27128	14	28
U14	LS10	7	14
U16	74159	12	24
U17	LS04	7	14

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C20	
CR2	
P9	E2
RN4	
U7	U4, U7,
TP10	
E2	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTOR VALUES ARE EXPRESSED IN OHMS.
2. ALL RESISTORS ARE 1/4W ± 5%.
3. ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.
4. ALL CAPACITORS ARE 100V.

5500215-02

Figure 9-10. Schematic Diagram, Microprocessor

A106
COUNT CHAIN
(2020136-03)

The Count Chain Assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 Converter (A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The Count Chain Assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces one or two IF output signals to be used for options at J3.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR5). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of the amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R47. The BCD outputs from U2 are slew-rate limited, and can only be seen on an oscilloscope after the counting ends and comes to rest. The carry output U2 pin 9 is an ECL level U2 signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascade output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the Count Chain Assembly. This circuit takes the 100 kHz reference signal that is coming from the Counter Interconnect Assembly (A100) and divides it

by 10,000 to give a 10 Hz (100 ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10 Hz rate for timing functions within the program.

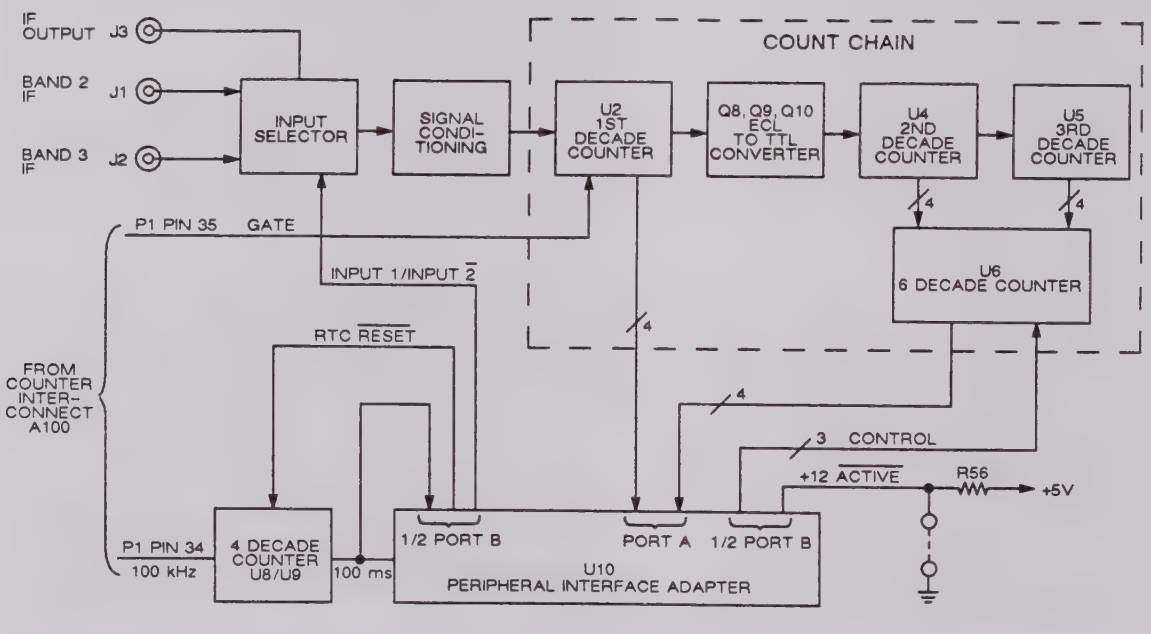


Figure 9-11. Count Chain Block Diagram

A106 COUNT CHAIN 2020136-03

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,TANTALUM	33µP		10V	2300015-00	5
C2		CAP,CER	.01µP	20%	100V	2150003-00	17
C3	C2						
C4	C1						
C5		CAP,MICA	10PF	5%	500V	2260012-00	1
C6		CAP,TANTALUM	10µF	20%	25V	2300029-00	4
C7	C2						
C8	C2						
C9		CAP,CER	.001µF	20%	100V	2150001-00	3
C10	C2						
C11		NOT USED					
C12	C9						
C13	C2						
C14	C6						
C15	C6						
C16	C2						
C17	C9						
C18		NOT USED					
C19		NOT USED					
C20	C1						
C21	C2						
C22	C1						
C23		NOT USED					
C24	C2						
C25	C2						
C26	C2						
C27	C2						
C28	C2						
C29	C1						
C30	C2						
C31	C2						
C32	C2						
C33	C2						
C34	C6						
CR1		DIODE,1N4148,FAST SWITCHING,GP				2704148-00	3
CR2		DIODE,1N5234,ZENER 6.2V				2705234-00	1
CR3	CR1						
CR4		DIODE,G00010,TUNNEL,SWITCHING				2710033-00	1
CR5		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
CR6	CR1						
J1		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	3
J2	J1						
J3	J1						
L1		NOT USED					
L2		INDUCTOR,1.0µH				3510003-00	1
Q1		XSTR,2N4959,PNP,RF				4704959-00	1
Q2		XSTR,MMBT3960,NPN SWITCHING				1410101-00	3
Q3	Q2						
Q4		XSTR,MPSH81,PNP,RF				4710010-00	1
Q5		XSTR,2N5179,PNP,RF GRADED-GRN				4710013-00	4
Q6		XSTR,NE73432B,NPN,RF				4710026-00	1
Q7	Q2						
Q8	Q5						
Q9	Q5						
Q10	Q5						
Q11		XSTR,2N4126,PNP,GP				4704126-00	2
Q12	Q11						

A106 COUNT CHAIN (Continued) 2020136-03

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R1		RES,CC	1.5K	1/4W	5%	4010152-00	2
R2		RES,CC	6.2K	1/4W	5%	4010622-00	2
R3		RES,M/OX	51	1/4W	2%	4130510-00	2
R4		RES,CC	5.1K	1/4W	5%	4010512-00	2
R5		RES,CC	2.7K	1/4W	5%	4010272-00	2
R6		RES,CC	51	1/4W	5%	4010510-00	1
R7		RES,M/OX	2K	1/4W	2%	4130202-00	3
R8		RES,CC	510	1/4W	5%	4010511-00	1
R9		RES,CC	5.6	1/4W	5%	4010569-00	5
R10	R5						
R11	R9						
R12		RES,M/OX	68	1/4W	2%	4130680-00	1
R13		RES,M/OX	43	1/4W	2%	4130430-00	
R14		RES,M/OX	3.9K	1/4W	2%	4130392-00	1
R15	R7						
R16	R4						
R17	R1						
R18	R2						
R19		RES,CC	100	1/4W	5%	4010101-00	1
R20		RES,M/OX	56	1/4W	2%	4130560-00	2
R21	R9						
R22	R20						
R23		RES,M/OX	360	1/4W	2%	4130361-00	1
R24	R9						
R25		RES,M/OX SEE NOTE 1	2.7K	1/4W	2%	4130272-00	1
R26		RES,M/OX	39	1/4W	2%	4130390-00	2
R27		RES,M/OX	200	1/4W	2%	4130201-00	3
R28		RES,M/OX	270	1/4W	2%	4130271-00	1
R29	R3						
R30		NOT USED					
R31		RES,CC	10	1/4W	5%	4010100-00	1
R32		RES,M/OX	47	1/4W	2%	4130470-00	1
R33		RES,M/OX	20	1/4W	2%	4130200-00	2
R34		RES,M/OX	510	1/4W	2%	4130511-00	1
R35	R9						
R36		RES,M/OX	1K	1/4W	2%	4130102-00	3
R37	R26						
R38		RES,CC	390	1/4W	5%	4010391-00	1
R39		RES,CC	10K	1/4W	5%	4010103-00	4
R40	R39						
R41	R39						
R42	R39						
R43		RES,M/OX	20K	1/4W	2%	4130203-00	4
R44	R43						
R45	R36						
R46	R43						
R47	R33	SEE NOTE 2					
R48	R43						
R49		RES,M/OX	240	1/4W	2%	4130241-00	1
R50	R27						
R51	R27						
R52	R36						
R53		RES,M/OX	430	1/4W	2%	4130431-00	1
R54	R7						
R55		RES,CC	1.8K	1/4W	5%	4010182-00	1
R56		RES,CC	4.7K	1/4W	5%	4010472-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	10
TP2	TP1						

NOTE 1 - SAT AS FOLLOWS: 2.4K OHMS MIN-3.3K OHMS MAX
NOTE 2 - R47 SAT AS FOLLOWS: 18 OHMS MIN-24 OHMS MAX

A106 COUNT CHAIN (Continued) 2020136-03

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
TP3	TP1			
TP4	TP1			
TP5	TP1			
TP6	TP1			
TP7	TP1			
TP8	TP1			
TP9	TP1			
TP10	TP1			
U1		IC,DUAL DIFF AMPL,LIN	3043049-00	1
U2		IC,SP8637B,HIGH SPEED DIVIDERS/10	3010637-00	1
U3		IC,LM741C,OP AMP	3040741-00	1
U4		IC,74LS196	3084196-00	1
U5		IC,74LS160	3084160-00	1
U6		IC,7031,CNTR,6-DECADE,UP,PMOS	3057031-00	1
U7		IC,74LS04	3087404-00	1
U8		IC,74LS490	3084490-00	2
U9	U8			
U10		IC,68B21P,PRPHL INTERFACE ADAPTER	3086821-00	1

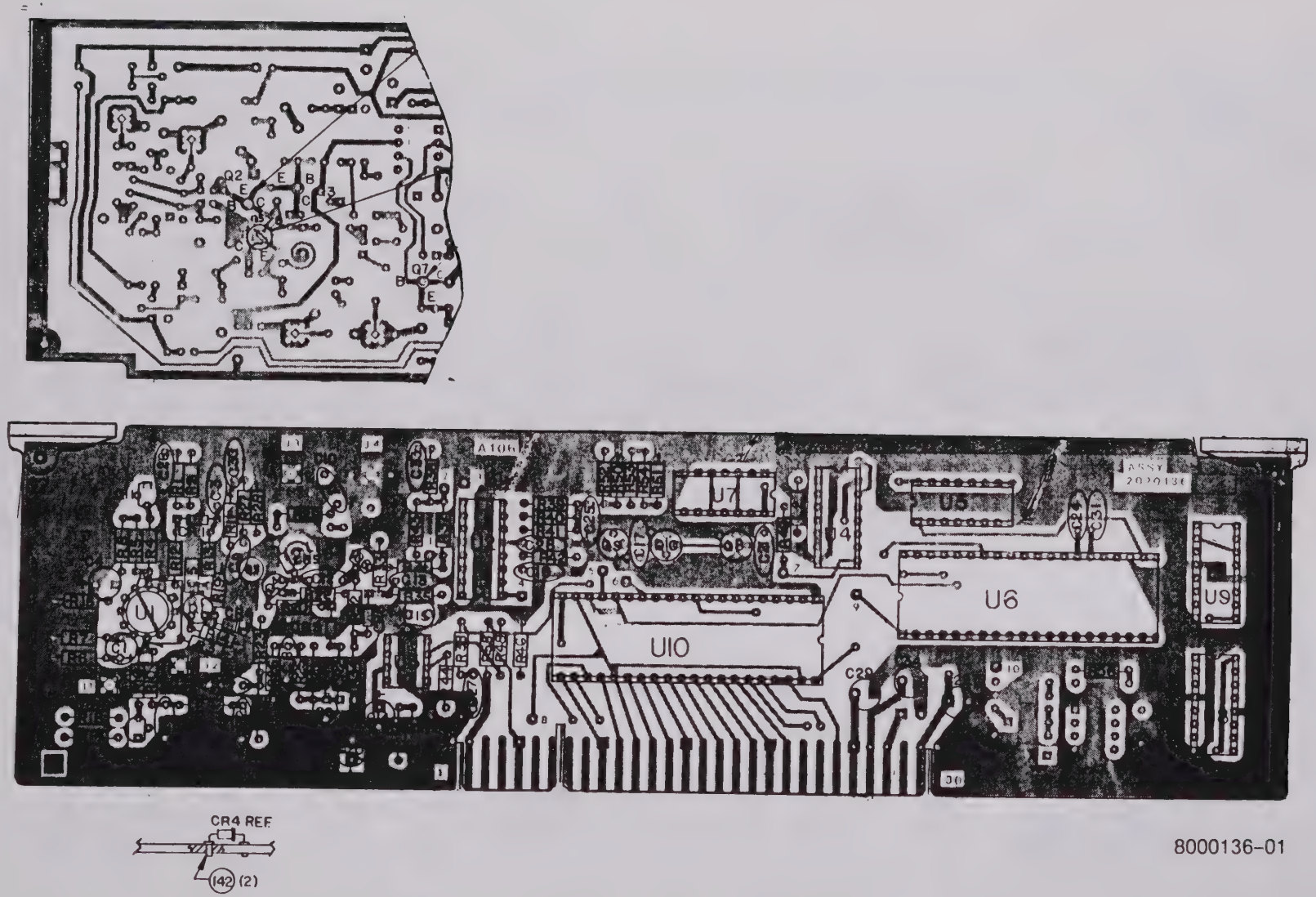
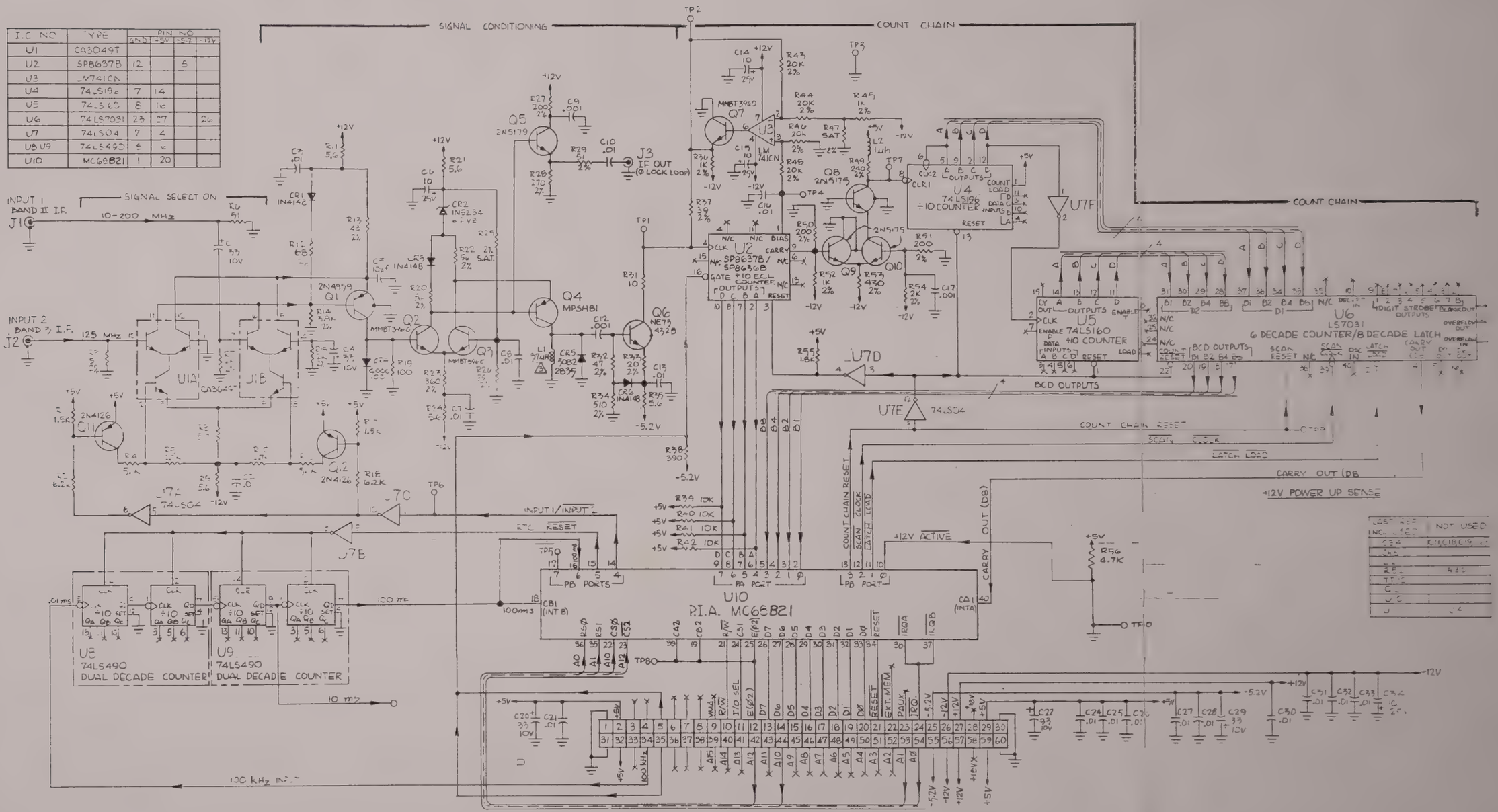


Figure 9–12. Component Locator, Count Chain

I.C NO	TYPE	PIN NO			
		GND	+5V	-5.2	-12V
U1	CA3049T				
U2	SPB637B	12		5	
U3	LM741CN				
U4	74LS193	7	14		
U5	74LS160	8	16		
U6	74LS7031	23	27		26
U7	74LS04	7	4		
U8 U9	74LS490	5	10		
U10	MC68B21	1	20		



5500136-03

Figure 9-13. Schematic Diagram, Count Chain

A107
GATE GENERATOR
(2020197-09)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 10 MHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel.

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int/Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1 V p-p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation). The output of U1 goes to J3 to be used by the microwave converter. The output of U1 also goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2.

GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 microsecond and 1 second. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 µsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100 kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6B clear (T0). The gate is initialized by setting U6B. This clears U6A and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6B (T3). The next clock sets U6A which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks, its output, pin 1, goes low. This sets U6B, which clears U6A, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6B (T9), which enables the gate to free-run again (T0). See Figure 9-14.

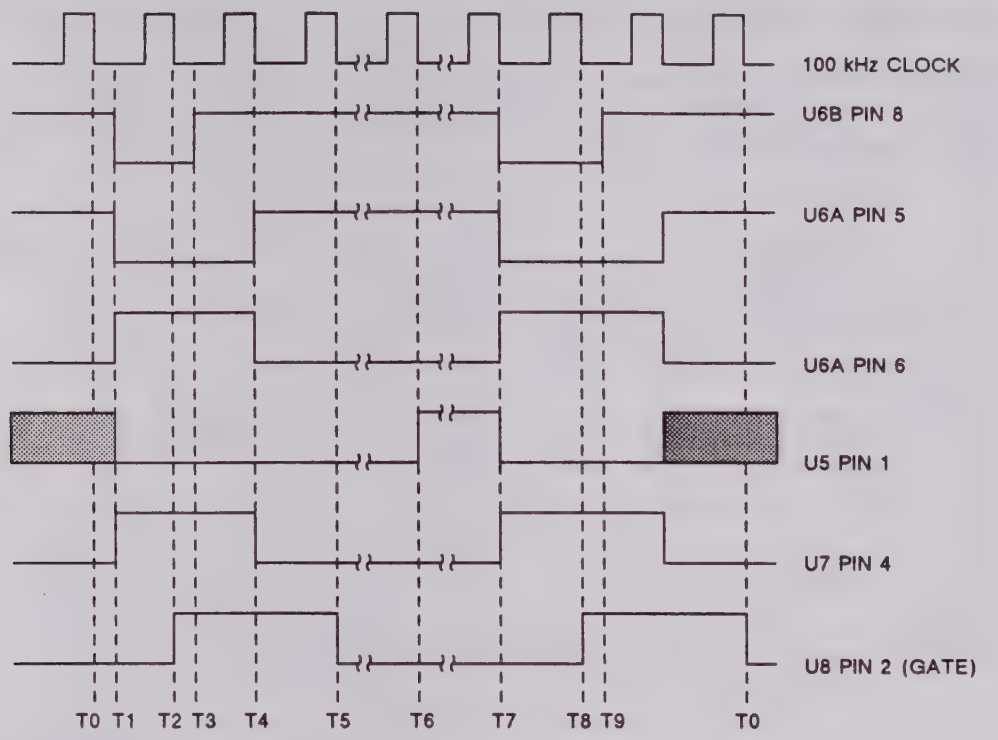


Figure 9-14. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ±200 micro amps, and the fine DAC (U4) has a range of +1.5 micro amps. The Power Meter Zero DAC (U3) is adjusted so that on step 1 U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0 volts, nulling any offsets in the power meter circuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), and 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the Option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100 mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. On counters without the power meter option, the amplitude is calculated to a 3 dB resolution. On counters with the power meter option, the amplitude is calculated to a resolution of 0.1 dB.

PERIPHERAL INTERFACE ADAPTER (PIA)

The Peripheral Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 1900 Hex to 1903 Hex. Peripheral Port A is at address 1900, and Peripheral Port B is at address 1902.

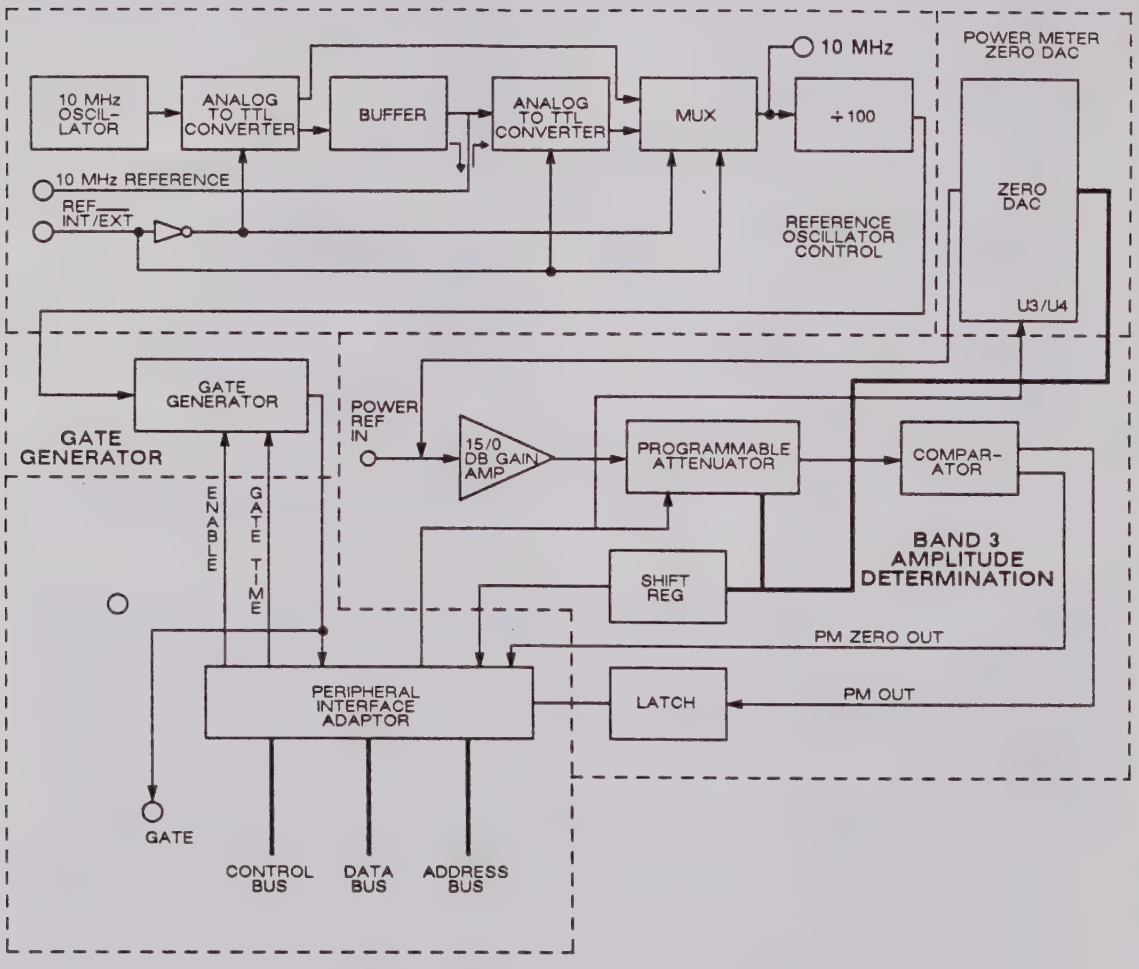


Figure 9-15. Gate Generator Block Diagram

A107 GATE GENERATOR 2020197-09

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,CER	.01µF	20%	100V	2150003-00	15
C2	C1						
C3		CAP,TANTALUM	33µF		10V	2300015-00	4
C4	C1						
C5	C1						
C6	C1						
C7	C1						
C8		CAP,MICA SEE NOTE 1	15PF	5%	500V	2260014-00	1
C9		CAP,TANTALUM	1µF		35V	2300008-00	1
C10		CAP,MICA	33PF	5%	500V	2260021-00	2
C11		CAP,MICA	100PF	5%	500V	2260034-00	1
C12	C10						
C13	C1						
C14	C1						
C15	C1						
C16		CAP,TANTALUM	10µF	20%	25V	2300029-00	2
C17	C1						
C18	C3						
C19	C3						
C20	C1						
C21	C1						
C22	C3						
C23	C1						
C24	C1						
C25	C16						
C26	C1						
CR1		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
CR2		DIODE,5082-2800,PSVT SCHOTTKY BARR				2710006-00	1
CR3		NOT USED					
CR4		DIODE,1N827,ZENER,6.2V				2700827-00	1
J1		CONN,PCB,RT ANGLE,3 PIN				2620132-00	2
J2		NOT USED					
J3	J1						
Q1		XSTR,2N4124,NPN,GP				4704124-00	4
Q2		XSTR,2N4126,PNP,GP				4704126-00	3
Q3	Q1						
Q4	Q2						
Q5	Q1						
Q6	Q2						
Q7	Q1						
Q8		XSTR,SD215,FET SW,N-CH,D-MOS				4710031-00	1
R1		RES,CC	10	1/4W	5%	4010100-00	2
R2		RES,CC	1K	1/4W	5%	4010102-00	2
R3		RES,CC	620	1/4W	5%	4010621-00	2
R4		RES,CC	2.2K	1/4W	5%	4010222-00	3
R5		RES,CC	220	1/4W	5%	4010221-00	2
R6		RES,CC	510	1/4W	5%	4010511-00	2
R7		RES,CC	200	1/4W	5%	4010201-00	1
R8		RES,CC	27	1/4W	5%	4010270-00	1
R9		RES,CC	300	1/4W	5%	4010301-00	1
R10		RES,CC	4.7K	1/4W	5%	4010472-00	6
R11	R1						
R12		RES,CC	2K	1/4W	5%	4010202-00	2
R13	R10						

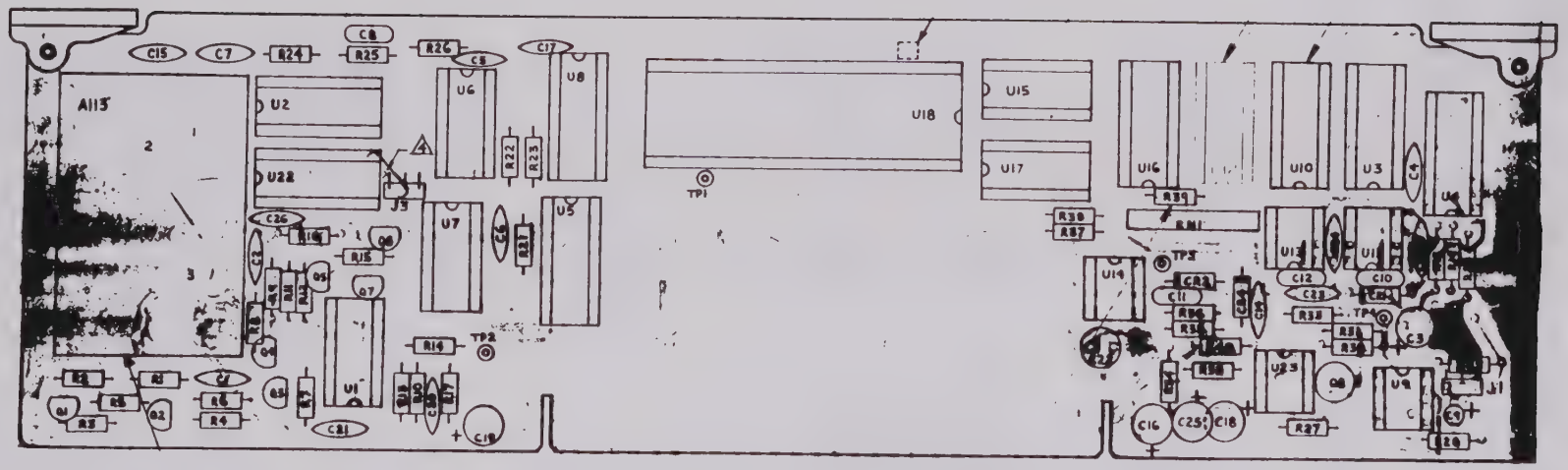
NOTE 1 - SAT AS FOLLOWS: 10PF MIN-36PF MAX

A107 GATE GENERATOR (Continued) 2020197-09

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R14	R4						
R15	R5						
R16	R6						
R17	R3						
R18		RES,M/OX	5.6K	1/4W	2%	4130562-00	1
R19		RES,M/OX	3.3K	1/4W	2%	4130332-00	1
R20		RES,M/OX	27	1/4W	2%	4130270-00	1
R21		RES,CC	2.7K	1/4W	5%	4010272-00	1
R22	R10						
R23	R10						
R24	R2						
R25	R12						
R26	R4						
R27		RES,M/OX	30K	1/4W	2%	4130303-00	1
R28		RES,M/OX	39K	1/4W	2%	4130393-00	1
R29		RES,MF	1.69K	1/10W	1%	4051691-00	1
R30		RES,MF	1.82K	1/10W	1%	4051821-00	1
R31		RES,MF	57.6K	1/10W	1%	4055762-00	1
R32		RES,CC	36K	1/4W	5%	4010363-00	1
R33		RES,CC	15K	1/4W	5%	4010153-00	1
R34		RES,M/OX	750	1/4W	2%	4130751-00	1
R35		RES,MF	6.19K	1/10W	1%	4056191-00	1
R36		RES,MF	100	1/8W	1%	4051000-00	1
R37	R10						
R38	R10						
R39		RES,M/OX	10K	1/4W	2%	4130103-00	2
R40	R39						
RN1		RES,NTWK	5X10K	0.3W	2%	4170005-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	4
TP2	TP1						
TP3	TP1						
TP4	TP1						
U1		IC,74LS132				3084132-00	1
U2		IC,74LS490				3084490-00	1
U3		IC,AD7524J,DAC,8-BIT,1/2 LSB				3057524-00	2
U4	U3						
U5		IC,5009,P-CHANNEL MOS DIVIDER				3035009-00	1
U6		IC,74LS74				3087474-00	2
U7		IC,74LS02				3087402-00	1
U8		IC,10131,ECL 10K,M-S FF				3110131-00	1
U9		IC,5534,OPNL AMP,LOW NOISE				3045534-00	1
U10		IC,AD7524J,DAC,8-BIT,1/2 LSB				3057524-00	1
U11		IC,LM308A,OPNL AMP/BUFFER				3040308-00	2
U12		NOT USED					
U13	U11						
U14		IC,LM393,VOLT COMP,LOW PWR				3050393-00	1
U15		IC,7407				3007407-00	1
U16		IC,4015,4-BIT STATIC SHIFT RGTR				3034015-00	1
U17	U6						
U18		IC,68B21P,PRPHL INTERFACE ADAPTER				3086821-00	1
U19		NOT USED					
U20		NOT USED					
U21		NOT USED					
U22		IC,74LS175				3084175-00	1
U23		IC,LM741C,OP AMP				3040741-00	1
XU1		CONN,SOCKET,DIP,14 PIN				2630015-00	5
XU2		CONN,SOCKET,DIP,16 PIN				2630016-00	9
XU3	XU2						

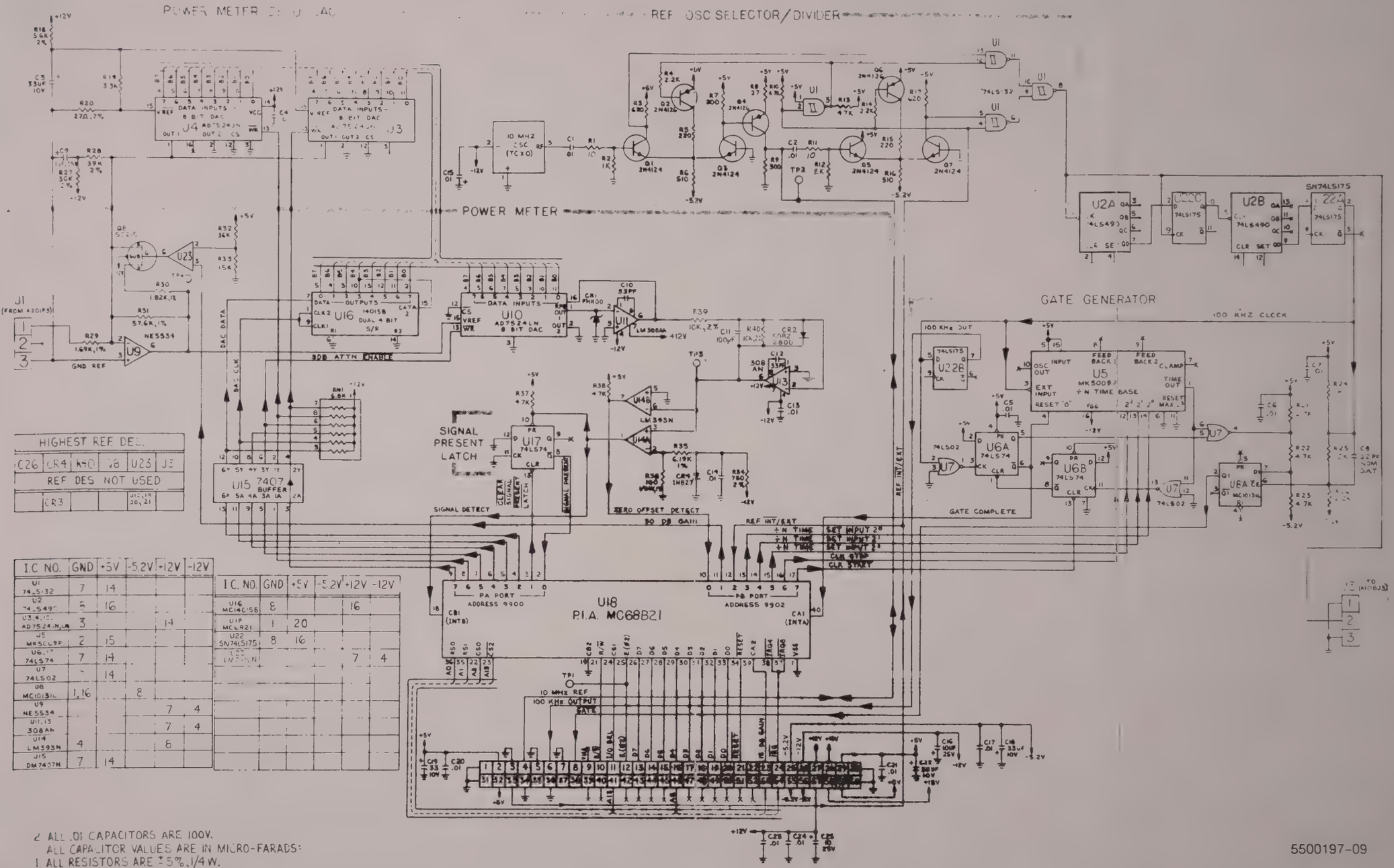
A107 GATE GENERATOR (Continued) 2020197-09

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
XU4	XU2			
XU5	XU2			
XU6	XU1			
XU7	XU1			
XU8	XU2			
XU9		CONN,SOCKET,DIP,8 PIN	2630014-00	5
XU10	XU2			
XU11	XU9			
XU12	XU2			
XU13	XU9			
XU14	XU9			
XU15	XU1			
XU16	XU2			
XU17	XU1			
XU18		CONN,SOCKET,DIP,40 PIN	2630022-00	1
XU19		NOT USED		
XU20		NOT USED		
XU21		NOT USED		
XU22	XU2			
XU23	XU9			



2020197-09

Figure 9-16. Component Locator, Gate Generator



I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	5	16			
U3,4,12 AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC1013L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U22 SN74LS175	8	16			
U23 LM336N				7	4

2. ALL .01 CAPACITORS ARE 100V.
   ALL CAPACITOR VALUES ARE IN MICRO-FARADS.
1. ALL RESISTORS ARE ±5%, 1/4 W.
   ALL RESISTOR VALUES ARE IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

5500197-09

Figure 9-17. Schematic Diagram, Gate Generator

A108
CONVERTER CONTROL
(2020200-07)

The Converter Control performs two major functions. One of the functions is to provide a precise YIG tuning current which is controlled by the microprocessor via P.I.A. U4. The other function is to phase lock the VCO in the microwave converter to a selected harmonic of a 50 kHz reference signal to provide a synthesized L.O. The converter control also permits the microprocessor to control the L.O. power amplifier and provides the microprocessor input for the I.F. threshold signal.

YIG FREQUENCY CONTROL DAC AND DRIVERS

The YIG tuning current is supplied by the YIG driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U2), summing amplifier (U1) and resistors to provide a total resolution of 14 bits. PA ports 0 and 1 of the P.I.A. (U4) are used to drive the 2 least significant bits of the DAC directly. A change in the least significant bit of the DAC corresponds to a YIG frequency change of 2 MHz. A voltage analog of YIG current appears across R25 and is compared to the DAC output at the summing junction of U3, with resistors R1 and R19.

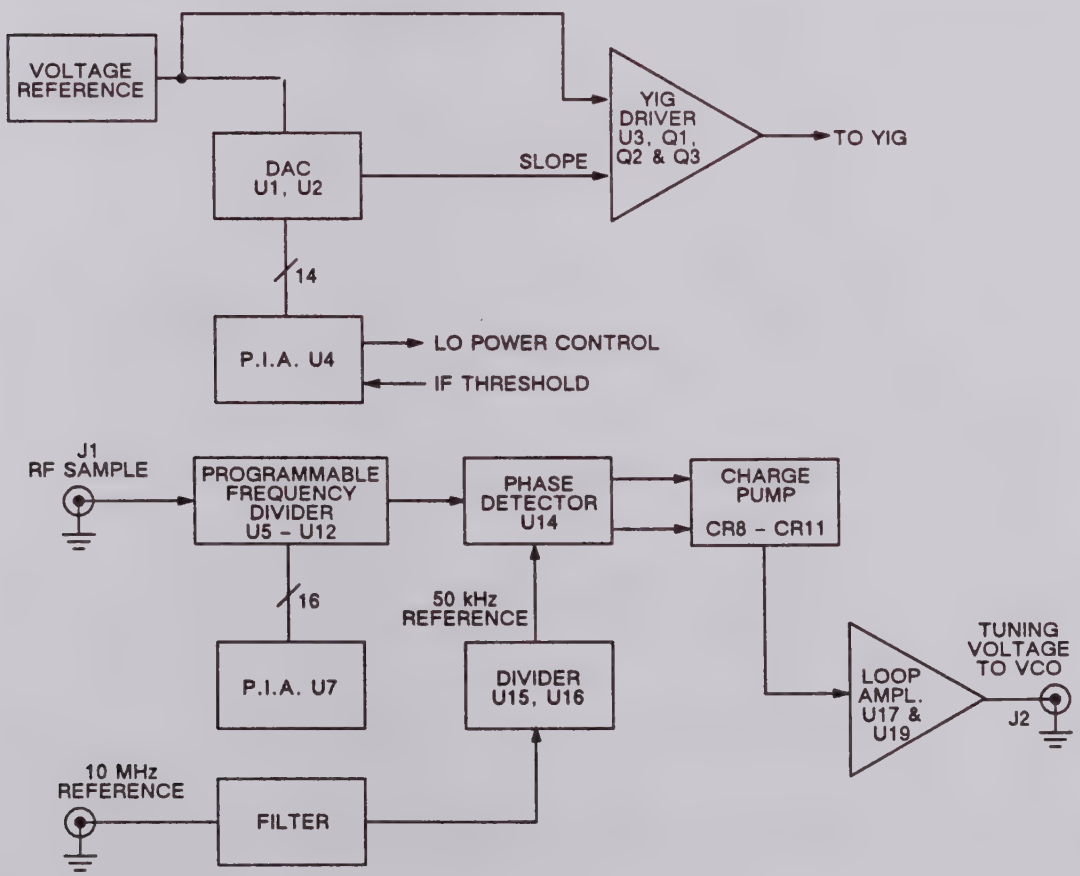


Figure 9-18. Converter Control Diagram

VCO CONTROL

The VCO control, together with the VCO, form a phase lock loop frequency synthesizer. The frequency range over which the synthesizer is used is from 370 MHz to 500 MHz.

An output of the VCO (via a buffer amplifier U2 on the Band 2 converter board) is applied to the programmable frequency divider (U5–U13). The programmable frequency divider is programmed by the microprocessor via P.I.A. U7. The output of the programmable frequency divider is compared to the 50 kHz reference (derived from a 10 MHz clock from the gate generator board) in the phase detector U14. A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump-down is U14, pin 2. Pump-down is normally high and goes low to reduce the VCO frequency. Pump-up is U18, pin 3. Pump-up is normally low and goes high to increase the VCO frequency. The outputs of the phase detector go to the charge pump, which converts then to a single tri-state output. The charge pump output is open with no pump command, sources current with pump-up, and sinks current with pump-down. The output of the charge pump is connected to the input of the loop amplifier U19 and U17. The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage.

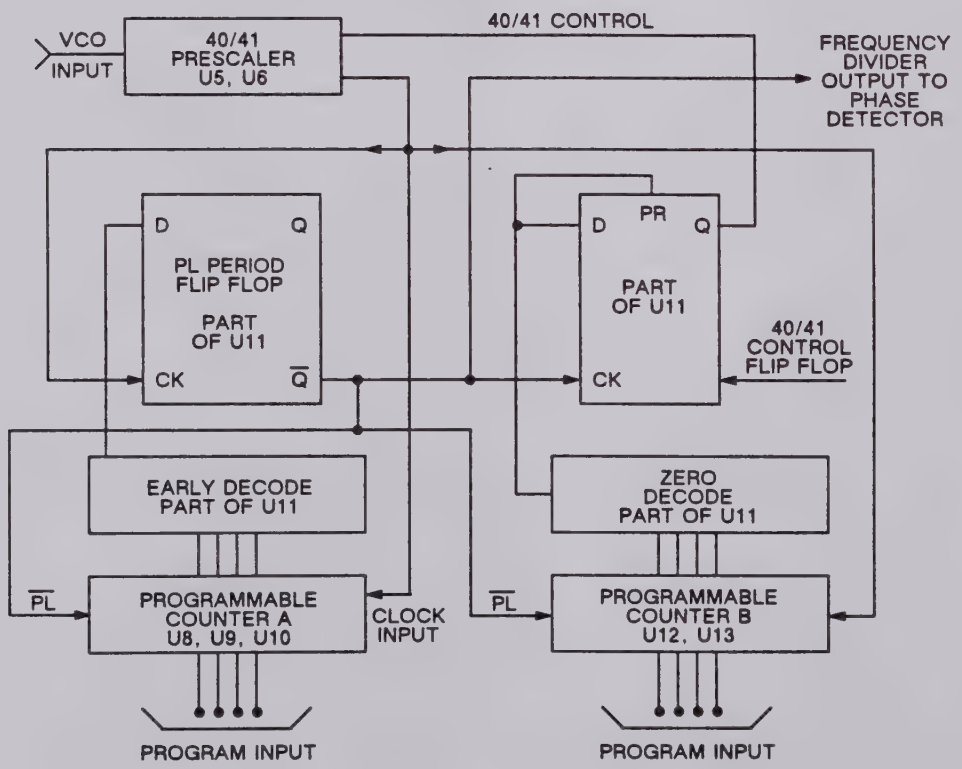


Figure 9-19. Programmable Frequency Divider Diagram

PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two modulus (divide number) prescaler (U5, U6) and two programmable counters (A & B). The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power Schottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters have been loaded with their respective program numbers from the PIA. The programmable counters each decrement 1 count for each output pulse from the prescaler. When programmable counter B (U12, U13) reaches the count of zero, the 40/41 control flip-flop (part of U11) changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A reaches the count of 2, the D input of the PL period flip-flop (part of U11) goes high, so that on the count of 1 the flip-flop changes state, which causes both programmable counters to be reloaded with their respective program numbers and the 40/41 control flip-flop to reset (prescaler in ÷ 41 state). The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ration of the programmable frequency divider N_d is:

$$N_d = 40\ (N \text{ counter A}) + N \text{ counter B}$$

with the condition that:

N counter B must not exceed N counter A

The weighting of the command bits is:

U9	P_1 – 400 MHz	U10 P_1	– 4 MHz
U9	P_0 – 200 MHz	U10 P_0	– 2 MHz
U8	P_3 – 160 MHz	U13 P_3	– 1.6 MHz
U8	P_2 – 80 MHz	U13 P_2	– 0.8 MHz
U8	P_1 – 40 MHz	U13 P_1	– 0.4 MHz
U8	P_0 – 20 MHz	U13 P_0	– 0.2 MHz
U10	P_3 – 16 MHz	U13 P_1	– 100 kHz
U10	P_2 – 8 MHz	U13 P_0	– 50 kHz

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A108 CONVERTER CONTROL 2020200-07

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,DISC,CER	.005µF	20%	100V	2150008-00	1
C2		CAP,CER	.01µF	20%	100V	2150003-00	14
C3		CAP,DISC,CER,X7R	.047µF	10%	50V	2150090-00	1
C4		CP,TANTALUM	1µF		35V	2300008-00	3
C5	C4						
C6	C2						
C7		CAP,CER	.001µF	20%	100V	2150001-00	3
C8	C4						
C9		CAP,TANTALUM	33µF		10V	2300015-00	2
C10	C7						
C11		CAP,SMD Z5U	.1µF	20%	50V	2100046-00	1
C12	C7						
C13	C2						
C14	C2						
C15	C2						
C16	C2						
C17	C2						
C18		CAP,TANTALUM	10µF	20%	25V	2300029-00	4
C19	C18						
C20	C9						
C21	C18						
C22	C2						
C23	C2						
C24	C2						
C25		CAP,DISC,CER,COG	560PF	5%	100V	2150029-00	2
C26		CAP,TANTALUM	47µF		35V	2300005-00	1
C27		CAP,CER	.022µF	15%	50V	2350027-00	1
C28	C18						
C29	C2						
C30		CAP,DISC,CER,COG	330PF	10%	100V	2150030-00	1
C31		CAP,TANTALUM	2.2µF	20%	16V	2300012-00	1
C32		CAP,MICA	82PF	5%	500V	2260032-00	2
C33	C2						
C34		CAP,MICA SEE NOTE 1	470PF	5%	500V	2250018-00	2
C35	C34						
C36		CAP,MICA SEE NOTE 2	300PF	5%	300V	2260045-00	1
C37		CAP,DISC,CER,X7R	.1µF	10%	50V	2150028-00	1
C38	C2						
C39		CAP,ML CER	2200PF	5%	100V	2150026-00	1
C40	C25						
C41	C2						
C42	C32						
CR1		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
CR2		DIODE,1N4758,ZENER 56V				2704758-00	1
CR3		DIODE,1N4148,FAST SWITCHING,GP				2704148-00	14
CR4		DIODE,1N827,ZENER,6.2V				2700827-00	1
CR5		DIODE,1N4001,PWR RECT				2704001-00	1
CR6	CR3						
CR7	CR3						
CR8	CR3						
CR9	CR3						
CR10	CR3						
CR11	CR3						
CR12	CR3						
CR13	CR3						

NOTE 1 - C34 SAT AS FOLLOWS: 430PF MIN-470PF MAX
NOTE 2 - SAT AS FOLLOWS: 82PF MIN-300PF MAX

A108 CONVERTER CONTROL (Continued) 2020200-07

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
CR14	CR3						
CR15	CR3						
CR16	CR3						
CR17	CR3						
CR18	CR3						
J1		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	2
J2	J1						
J3		CONN,PCB,RT ANGLE,3 PIN				2620132-00	1
L1		INDUCTOR,100µH				3520007-00	1
L2		INDUCTOR,1µH				3510018-00	1
L3		INDUCTOR,4700µH				3510017-00	2
L4	L3						
R1		RES,PRON	8.00K	3/20W	1%	4120022-00	1
R2		RES,CC	4.7K	1/4W	5%	4010472-00	1
R3		RES,CC	1K	1/4W	5%	4010102-00	6
R4		NOT USED					
R5		RES,M/OX	390	1/4W	2%	4130391-00	2
R6		NOT USED					
R7		NOT USED					
R8	R3						
R9		NOT USED					
R10		NOT USED					
R11		NOT USED					
R12		NOT USED					
R13	R5						
R14		RES,CC	750	1/4W	5%	4010751-00	1
R15		RES,CC	820K	1/4W	5%	4010824-00	1
R16	R3						
R17		RES,M/OX	1.6K	1/4W	2%	4130162-00	1
R18		RES,CC	160K	1/4W	5%	4010164-00	1
R19		RES,PREC	3.01K	1/10W	1%	4120020-00	1
R20		RES,CC	10K	1/4W	5%	4010103-00	3
R21		RES,CC	82K	1/4W	5%	4010823-00	1
R22	R20						
R23	R20						
R24	R3						
R25		RES,WW	5	7W	1%	4110003-00	1
R26		RES,CC	2.7K	1/4W	5%	4010272-00	1
R27		RES,SMD	1K	1/8W	1%	4220009-00	1
R28		RES,CC	390	1/4W	5%	4010391-00	3
R29	R28						
R30	R28						
R31	R3						
R32		RES,CC	100	1/4W	5%	4010101-00	3
R33	R3						
R34		RES,CC	2.4K	1/4W	5%	4010242-00	1
R35	R32						
R36		RES,CC	220K	1/4W	5%	4010224-00	1
R37	R32						
R38		RES,CC SEE NOTE 3	4.3K	1/4W	5%	4010432-00	1
R39		RES,CC	2K	1/4W	5%	4010202-00	1
R40		RES,CC	51	1/4W	5%	4010510-00	1
R41		RES,CC	1.5M	1/4W	5%	4010155-00	1
R42		RES,CC	300	1/4W	5%	4010301-00	1
R43		RES,CC	8.2K	1/4W	5%	4010822-00	1
R44		RES,CC	51K	1/4W	5%	4010513-00	2
R45		RES,CC	5.1K	1/4W	5%	4010512-00	1

NOTE 3 - SAT AS FOLLOWS: 3.9K MIN-4.7K MAX

A108 CONVERTER CONTROL (Continued) 2020200-07

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
R46	R44			
R47		RES,CC 3.3K 1/4W 5%	4010332-00	1
R48		RES,SMD 51.5 1/8W 1%	4220002-00	1
S1		SWITCH,DIP, SPDT 1 POSN	4540007-00	1
TP1		CONN,PCB,.040D PIN,GOLD	2620032-00	14
TP2	TP1			
TP3	TP1			
TP4	TP1			
TP5		NOT USED		
TP6	TP1			
TP7	TP1			
TP8		NOT USED		
TP9	TP1			
TP10	TP1			
TP11	TP1			
TP12	TP1			
TP13	TP1			
TP14	TP1			
TP15	TP1			
TP16	TP1			
U1		IC,OP-16F,OPNL AMPL,JFET INP,TP-99	3041016-00	1
U2		IC,7541C-2,12-BIT MULTIPLYING DAC	3050012-00	1
U3		IC,LM741C,OP AMP	3040741-00	1
U4		IC,68B21P,PRPHL INTERFACE ADAPTER	3086821-00	2
U5		IC,12013,ECL 2-MODULOUS PRESCALER	3112013-02	1
U6		IC,10131,ECL 10K,M-S FF	3110131-00	1
U7	U4			
U8		IC,74LS192	3084192-00	4
U9	U8			
U10	U8			
U11		IC,12014,COUNTER CONTROL LOGIC	3112014-00	1
U12		IC,74LS193	3084193-00	1
U13	U8			
U14		IC,MC4044,PHASE FREQ DET	3014044-00	1
U15		IC,74LS175	3084175-00	1
U16		IC,74LS490	3084490-00	1
U17		IC,TL071C,OPNL AMPL,LOW NOISE	3040071-00	2
U18		IC,74LS00	3087400-00	1
U19	U17			
XU1		CONN,IC PIN(MINISERT)	2620054-00	11
XU2		CONN,SOCKET,DIP,18 PIN	2630017-00	1
XU3		NOT USED		
XU4		CONN,SOCKET,40 PIN	2630022-00	2
XU5		NOT USED		
XU6		CONN,SOCKET,DIP,16 PIN	2630016-00	9
XU7	XU4			
XU8	XU6			
XU9	XU6			
XU10	XU6			
XU11	XU6			
XU12	XU6			
XU13	XU6			
XU14		CONN,SOCKET,DIP,14 PIN	2630015-00	2
XU15	XU6			
XU16	XU6			
XU17		NOT USED		
XU18	XU14			
XQ1	XU1			

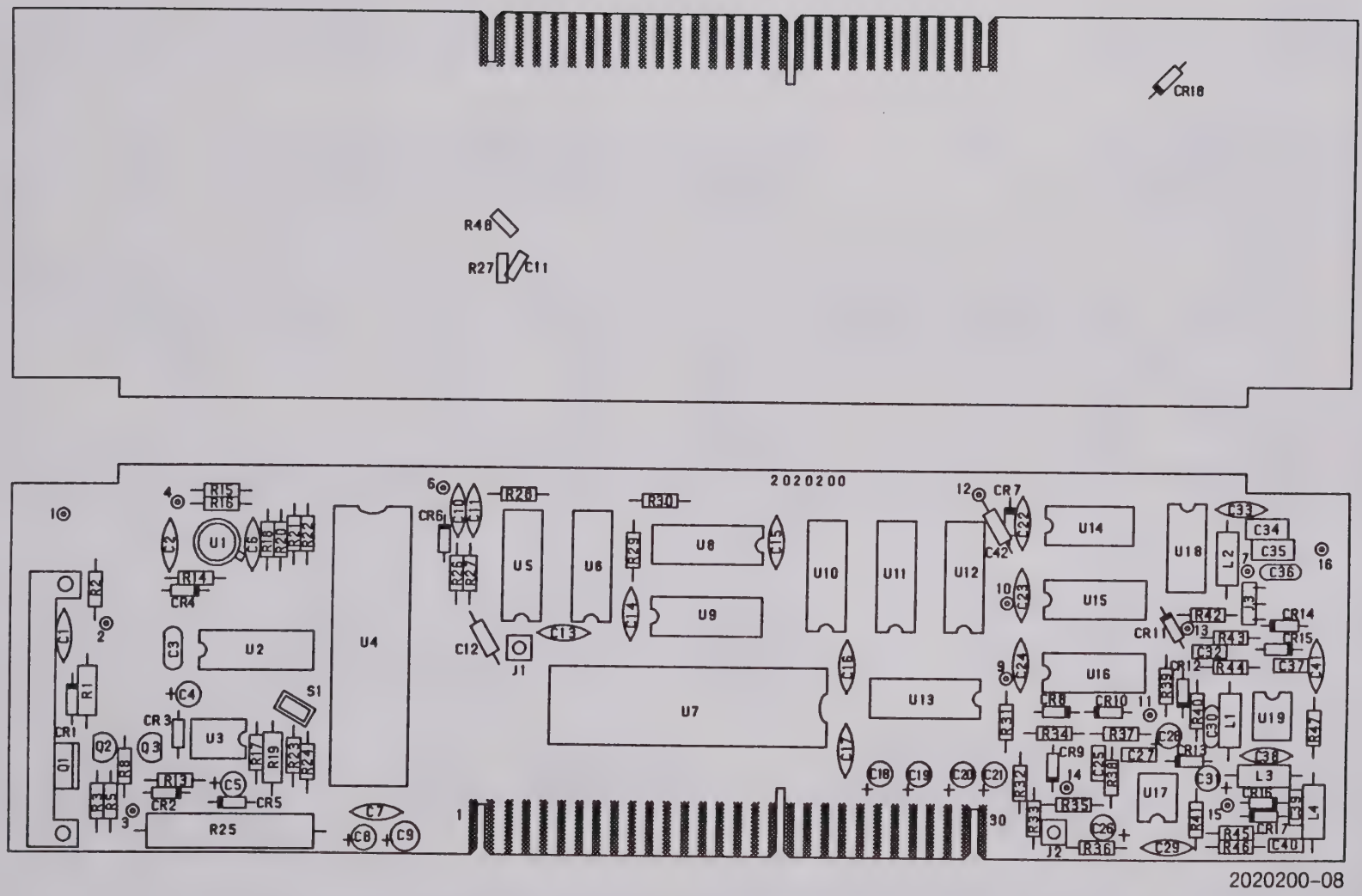


Figure 9-20. Component Locator, Converter Control

FREQUENCY CONTROL D.A.C.

VOLTAGE REF

YIG DRIVER

LOOP AMP

CHARGE PUMP

PHASE DET

PROGRAMMABLE COUNTER

40/41 PRESCALER

L.O POWER CONTROL

IF THRESHOLD

S1 PROTECT

TO YIG

I.C. Nº	TYPE	PIN NO. GND	-5.2	+5	-12	+12
U1	OP16FJ	—	—	—	4	7
U2	HS7541	8	—	—	—	16
U3	LM741CN	—	—	—	4	7
U4, U7	MC68B21	1	—	20	—	—
U5	MC12013	8	—	1,16	—	—
U6	MC10131	8	—	1,16	—	—
U8, U9	74LS192	8	—	16	—	—
U10, U13	74LS192	8	—	16	—	—
U11	MC12014	8	—	16	—	—
U14	MC4044	7	—	14	—	—
U15	74LS175	8	—	16	—	—
U16	74LS490	8	—	16	—	—
U17, U19	TL071CP	—	—	—	4	7
U18	74LS00	7	—	14	—	—

LAST RE USED	NOT USED
C42	R4, 6, 7, 8,
CR17	10, 11, 12,
J3	
L4	
Q3	
R48	
TP16	TP8
U19	

△4 S.A.T. RANGE 430 PF MIN - 470 PF MAX.

3. ALL DIODES ARE IN4148.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS. ALL .01 UF CAPACITORS ARE 100V.

1. ALL RESISTORS ARE ¼W, 5%, AND EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

5500200-07

Figure 9-21. Schematic Diagram, Converter Control

A109
BAND 2 CONVERTER
(2020139-07)

The Band 2 Converter accepts Band 1 and Band 2 RF signals from the front panel, and local oscillator (LO) signal from the Band 3 Converter (A203). The appropriate signal is selected and processed to produce an IF signal between 10 Hz and 200 MHz. The IF signal output is sent to the Count Chain board (A106), and lock information is routed through the PIA (peripheral interface adapter) U2 to the Microprocessor (A105).

IMPEDANCE CONVERTER

Band 1 input from the front panel enters the converter at J6 and is terminated by R75. The signal is coupled to the input of a field effect transistor (FET) amplifier (Q15) through an RC network (R73, C42). Two limiter diodes (CR4, CR5) protect the FET against large input signals. The FET is a source follower with slightly less than unity gain. The FET drives a buffer amplifier (Q14) which has enough gain to increase the impedance converter overall gain to near unity. A decoupling capacitor (C39) controls the amplifier low frequency cutoff, and C41 provides high frequency peaking to keep the gain flat to frequencies above 100 MHz.

SIGNAL SELECT

The output of the impedance converter circuit drives one input of the signal select circuitry. Signal selection is made by enabling one of three differential amplifiers, U4A, U4B, or U5A. When Band 1 is selected, a logic high signal on the PIA (U2 pin 2) turns on Q16. Q16 biases on the current source in U4A. This current source generates an 11 mA current which is split between the two differential amplifier transistors in U4A. The currents from pins 5 and 6 flow through matched collector loads (R94, L7/R95, L8). R94 and R95 are equal, and are selected for the proper low frequency gain during board alignment. Inductors L7 and L8 provide peaking to give an approximate flat gain through 200 MHz. Diodes CR9 and CR10 provide limiting on very strong signals to prevent the next stage from being overdriven.

The next stage is a differential amplifier similar to U4A, but it is driven differentially. To generate a single ended output signal, one output of U5B (Pin 12) is passed through a current mirror (Q18). The output of the current mirror is then added to the second output of U5B (pin 11) at J5. The load for this stage is a 51 ohm resistor located on the A106 Count Chain board in order to terminate the coax for RF signals. In the quiescent state, the current from Q18 equals the collector current of the differential amplifier U5B, and the output current is zero. When a signal is applied, the current will be unbalanced to generate a signal at the load resistor. To provide frequency compensation of the current mirror, an RC network (R108, C54) is connected between the emitter of Q18 and ground.

BAND 1 LOCK DETECTOR

The output signal at J5 is coupled to detector CR12. Amplifier U6 is a threshold comparator that will produce a logic low signal when the IF output from J5 is more than -6 dBm. The output of U6 goes through a resistor divider network to generate a 5V TTL logic signal for the PIA. R90 provides about 1 dB of positive feedback at threshold level to prevent erratic output from the comparator.

ISOLATION AMPLIFIER

The Band 2 input signal enters on J4. This RF signal is terminated in 50 ohms by the combination of R1 and the input impedance of the amplifier. The input signal level is detected by CR1, filtered by C3, and applied to one input of the Band 2 lock detector (U1).

The isolation amplifier is a common base amplifier with a gain of –10 dB. An input signal range of +10 to –20 dBm is translated to a 0 to –30 dBm range into the mixer so the mixer will be in its linear range for all signal input levels. The amplifier peaks slightly near 1 GHz to overcome an increase in mixer conversion loss at these frequencies.

MIXER OPERATION

The local oscillator (LO) is applied to the IF terminal and the IF is removed from the LO terminal. This swap allows the mixer (MX1) to be unbalanced and act as a low loss attenuator for signals between 10 MHz and 200 MHz where no mixing is necessary. The mixer has a nominal 400 MHz LO for signals between 200 MHz and 600 MHz; and has a nominal 800 MHz LO for signals between 600 MHz and 1 GHz. A 980 MHz LO allows operation with input signals to 1160 MHz.

IF AMPLIFIER

The output of the mixer drives an IF amplifier through a 7 section, 200 MHz low-pass filter. The IF amplifier is a "feedback pair" amplifier whose gain is stabilized by feedback, to be equal to 24 dB. Inductor L6 is used to extend the high frequency response to 200 MHz. The 1 pF capacitor (C26) between R34 and R35 is a low pass filter to reduce the 1200 to 1500 MHz LO harmonics that reach the IF amplifier.

BAND 2 LOCK DETECTOR

The IF amplifier output goes to the signal select circuit and to the Band 2 Lock Detector. The Band 2 Lock Detector has a voltage proportional to the IF level on the positive input, and a voltage proportional to the RF signal on the negative input. The conversion gain from RF input to IF amplifier output is a +6 dB for all valid signals, and less than –6 dB for all spurious signals. The output of U1 is positive only when a valid IF signal is present. A small offset is added by R12 and R13 to guarantee a non lock condition when no signal is present. Resistor R9 provides about 1 dB of positive feedback to prevent erratic output from noise at the point of threshold.

LO BUFFER

The VCO signal from the Band 3 Converter (A201A, J2) enters on J1. The signal goes through a 6 dB attenuator (R111, R112, R114), and a low pass filter (L1, C63, C64) to attenuate high order harmonics, and is terminated by a 51 ohm resistor (R16). Two high input impedance signal splitters (Q2, Q3) get their input signals from R16. Q2 and Q3 operate on the same basic principal. One output is taken from the emitter (acting as an emitter follower) that provides unity gain for the input signal. The AC terminating impedance on the emitter is adjusted to be 50 ohms so that amplifier will act as a unity gain amplifier for the 50 ohm load that terminates the collector when a coax cable is connected. Q2 has an additional transformer (T1) in its collector lead to increase the signal output to J3 by about 4 dB.

DIVIDE-BY-TWO

The emitter output of Q3 drives the input of a divide-by-two IC (U3). The impedance is held at 50 ohms by two terminating/biasing resistors (R61, R62). The resistors keep the input bias to U3 below the emitter-coupled logic (ECL) low level (approx. -2.0V). The microprocessor enables self-test by putting a low level signal on pin 5 of the PIA (U2). This turns on Q13, and raises the voltage at U3 pin 7 to the center of an ECL signal (approx. -1.2V). This allows U3 to divide the input signal by two. The output of U3 goes to the signal select circuits.

LO SELECT

The signal from the emitter of Q2 drives the LO select circuitry. The LO provides one (of three) signals to the mixer (MX1). In Band 2A a bias current is generated to unbalance the mixer and allow signals below 190 MHz to pass. In Band 2B a 370 MHz or 425 MHz LO signal is generated that will mix with signals of 200 to 600 MHz, and provide the 10 to 200 MHz IF signal desired. In Band 2C a 750 MHz, 850 MHz or 980 MHz LO signal is generated to mix with input signals between 600 MHz and 1160 MHz to provide the desired IF signal.

In Band 2A, the 3 mA current to bias mixer MX1 is generated when Q12 is turned on by the PIA, to apply +12V to MX1 through R57. This will allow signals to pass that are less than the cutoff frequency of the low pass filter (200 MHz). The LO signal to mixer MX2 from Q2 is not allowed to pass MX2 because of the inherent balance of the mixer. No signal can enter pin 2 of MX2 because Q7 has been saturated, removing bias from buffer Q5, and shunting any RF signals to ground.

When Band 2B is selected, Q12 is turned off thus balancing mixer MX1; Q6 is turned on to unbalance mixer MX2. With MX2 unbalanced, the LO signal from Q2 can pass through MX2 and be amplified by Q10 and Q11, and be applied to mixer MX1.

When Band 2C is selected both Q6 and Q12 are off, and both mixers are balanced. In this mode Q7 is shut off and an LO signal is applied to pin 1 and 2 of MX2. The sum output of MX2 is selected by a DC blocking capacitor (C31). This sum (that is, two times the incoming LO frequency) is amplified by Q10 and Q11 and applied to MX1.

The Q10 and Q11 amplifier is a series shunt pair. Q10 applies most of the RF input signal across the emitter resistor R47. This determines the transistor emitter current, which will be the collector current if the output is terminated in a low impedance. Q11 is used as a current-to-voltage converter. The output voltage of this converter is the product of the input current times the feedback resistor (R51). Since the input of this stage is a summing junction, it appears very close to zero ohms to the previous stage, Q10. The voltage gain of the two transistors can be approximated by R51/R47, which is about 3 or 10 dB. Since the gain required at 800 MHz is slightly greater than required at 400 MHz, a low pass matching network (consisting of L2 and C20) peaks the output signal current to MX1 at 800 MHz. The remaining components around Q10 and Q11 are used to bias the transistors. Shunt biasing is used to provide collector bias voltages of 3.4V for Q10, and 4.7V for Q11.

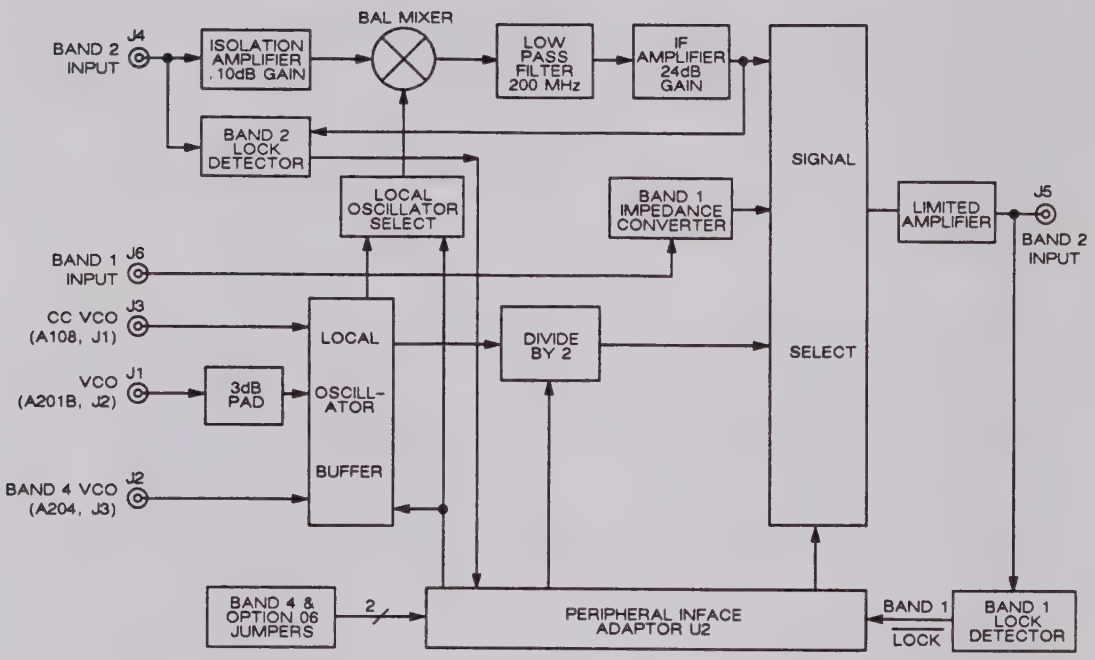


Figure 9-22. Band 2 Converter Block Diagram

A109 BAND 2 CONVERTER 2020139-07

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ML CER	.01µF	10%	100V	2150014-00	9
C2	C1						
C3		CAP,ML CER	.001µF	10%	100V	2150015-00	11
C4	C1						
C5	C1						
C6	C1						
C7		CAP,MICA	100PF	5%	500V	2260034-00	3
C8		CAP,CER	.001µF	20%	100V	2150001-00	8
C9		CAP,CER	.01µF	20%	100V	2150003-00	11
C10	C8						
C11	C8						
C12	C7						
C13	C8						
C14	C7						
C15	C3						
C16	C3						
C17	C3						
C18	C3						
C19	C8						
C20		CAP,MICA	1PF	100%	500V	2260005-00	2
C21		CAP,MICA SEE NOTE 1	18PF	5%	500V	2260015-00	2
C22		CAP,MICA SEE NOTE 2	33PF	5%	500V	2260021-00	2
C23	C22						
C24		CAP,MICA SEE NOTE 3	27PF	5%	500V	2260019-00	1
C25	C1						
C26	C20						
C27		NOT USED					
C28	C1						
C29	C9						
C30	C1						
C31	C3						
C32	C3						
C33	C1						
C34	C3						
C35	C3						
C36	C3						
C37	C9						
C38	C3						
C39		CAP,TANTALUM	100µF			2300024-00	1
C40	C9						
C41		CAP,MICA	22PF	5%	500V	2260017-00	1
C42		CAP,MICA	47.0PF	5%	500V	2260004-00	1
C43		CAP,TANTALUM	33µF		10V	2300015-00	6
C44	C9						
C45	C43						
C46	C8						
C47	C9						
C48	C9						
C49	C9						
C50		CAP,TANTALUM	10µF	20%	25V	2300029-00	3
C51	C43						
C52	C9						
C53	C9						
C54	C21						

NOTE 1 - C21 SAT AS FOLLOWS: 12PF MIN-24PF MAX
NOTE 2 - SAT AS FOLLOWS: 24PF MIN-39PF MAX
NOTE 3 - SAT AS FOLLOWS: 22PF MIN-36PF MAX

A109 BAND 2 CONVERTER (Continued) 2020139-07

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
C55	C8			
C56	C8			
C57	C50			
C58	C43			
C59	C9			
C60	C43			
C61	C50			
C62	C43			
C63		CAP,MICA 8PF 13% 500V	2260011-00	2
C64	C63			
CR1		DIODE,1SS16,MIXER,UHF SCHOTTKY BAR	2710038-00	3
CR2		NOT USED		
CR3	CR1			
CR4		DIODE,1N4148,FAST SWITCHING,GP	2704148-00	3
CR5	CR4			
CR6		NOT USED		
CR7		NOT USED		
CR8		NOT USED		
CR9		NOT USED		
CR10		NOT USED		
CR11	CR4			
CR12	CR1			
J1		CONN,COAX PC RCPT,SNAP NANOHEX	2610038-00	6
J2	J1			
J3	J1			
J4	J1			
J5	J1			
J6	J1			
L1		NOT USED		
L2		NOT USED		
L3		NOT USED		
L4		NOT USED		
L5		NOT USED		
L6		INDUCTOR, .47µH	3510006-00	1
MX1		MIXER,BALANCE,DOUBLE	2030016-00	2
MX2	MX1			
Q1		XSTR,BFR90,NPN,HIGH FREQ	4710030-00	9
Q2	Q1			
Q3	Q1			
Q4		XSTR,2N4124,NPN,GP	4704124-00	1
Q5	Q1			
Q6		XSTR,2N4126,PNP,GP	4704126-00	7
Q7	Q1			
Q8	Q1			
Q9	Q1			
Q10	Q1			
Q11	Q1			
Q12	Q6			
Q13	Q6			
Q14		XSTR,PNP RF,MOD (MF 4710045-00)	5280047-00	2
Q15		XSTR,2N4416,JFET,N-CH	4704416-00	1
Q16	Q6			
Q17	Q6			
Q18	Q14			
Q19	Q6			
Q20	Q6			

A109 BAND 2 CONVERTER (Continued) 2020139-07

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R1		RES,CC	150	1/8W	5%	4000151-00	1
R2		RES,MF	75.0	1/8W	1%	4067509-00	1
R3		RES,M/OX	1.1K	1/4W	2%	4130112-00	1
R4		RES,M/OX	820	1/4W	2%	4130821-00	3
R5		RES,CC	33	1/8W	5%	4000330-00	1
R6		RES,CC	51	1/8W	5%	4000510-00	1
R7		RES,CC	10K	1/4W	5%	4010103-00	3
R8		RES,M/OX	8.2K	1/4W	2%	4130822-00	2
R9		RES,M/OX	30K	1/4W	2%	4130303-00	1
R10		RES,M/OX	43K	1/4W	2%	4130433-00	2
R11		RES,CC	43K	1/4W	5%	4010433-00	1
R12		RES,M/OX SEE NOTE 4	15K	1/4W	2%	4130153-00	1
R13		RES,MF	12.1	1/8W	1%	4061219-00	1
R14		RES,CC	36	1/4W	5%	4010360-00	1
R15		RES,CC	11	1/4W	5%	4010110-00	2
R16		RES,MF	51.1	1/8W	1%	4065119-00	2
R17		RES,CC	1K	1/4W	5%	4010102-00	5
R18		RES,CC	100	1/4W	5%	4010101-00	2
R19	R15						
R20	R17						
R21		RES,CC	220	1/4W	5%	4010221-00	2
R22		RES,CC	20K	1/4W	5%	4010203-00	1
R23		RES,CC	820	1/4W	5%	4010821-00	2
R24		RES,CC	10	1/4W	5%	4010100-00	11
R25		RES,M/OX	750	1/4W	2%	4130751-00	2
R26		RES,CC	11K	1/4W	5%	4010113-00	3
R27		RES,M/OX	4.7K	1/4W	2%	4130472-00	1
R28		RES,MF	33.2	1/8W	1%	4063329-00	2
R29		RES,CC	4.7K	1/4W	5%	4010472-00	2
R30	R26						
R31		RES,CC	8.2K	1/4W	5%	4010822-00	2
R32	R7						
R33	R7						
R34		RES,MF	27.4	1/8W	1%	4062749-00	1
R35		RES,MF	24.3	1/8W	1%	4062439-00	1
R36	R24						
R37		RES,CC	10	1/8W	5%	4000100-00	1
R38	R17						
R39	R4						
R40	R4						
R41	R24						
R42	R16						
R43	R24						
R44		RES,CC	910	1/4W	5%	4010911-00	1
R45		RES,CC	3.9K	1/4W	5%	4010392-00	3
R46		RES,CC	27K	1/4W	5%	4010273-00	1
R47	R28						
R48		RES,CC	3.3K	1/4W	5%	4010332-00	1
R49		RES,CC	390	1/4W	5%	4010391-00	1
R50		RES,CC	13K	1/4W	5%	4010133-00	1
R51		RES,MF	121	1/8W	1%	4061210-00	1
R52	R24						
R53	R31						
R54	R26						
R55	R25						
R56	R24						
R57		RES,M/OX SEE NOTE 5	4.3K	1/4W	2%	4130432-00	1
R58	R17						

NOTE 4 - SAT AS FOLLOWS: 12K MIN-24K MAX
NOTE 5 - SAT AS FOLLOWS: 3.9K MIN-4.7K MAX

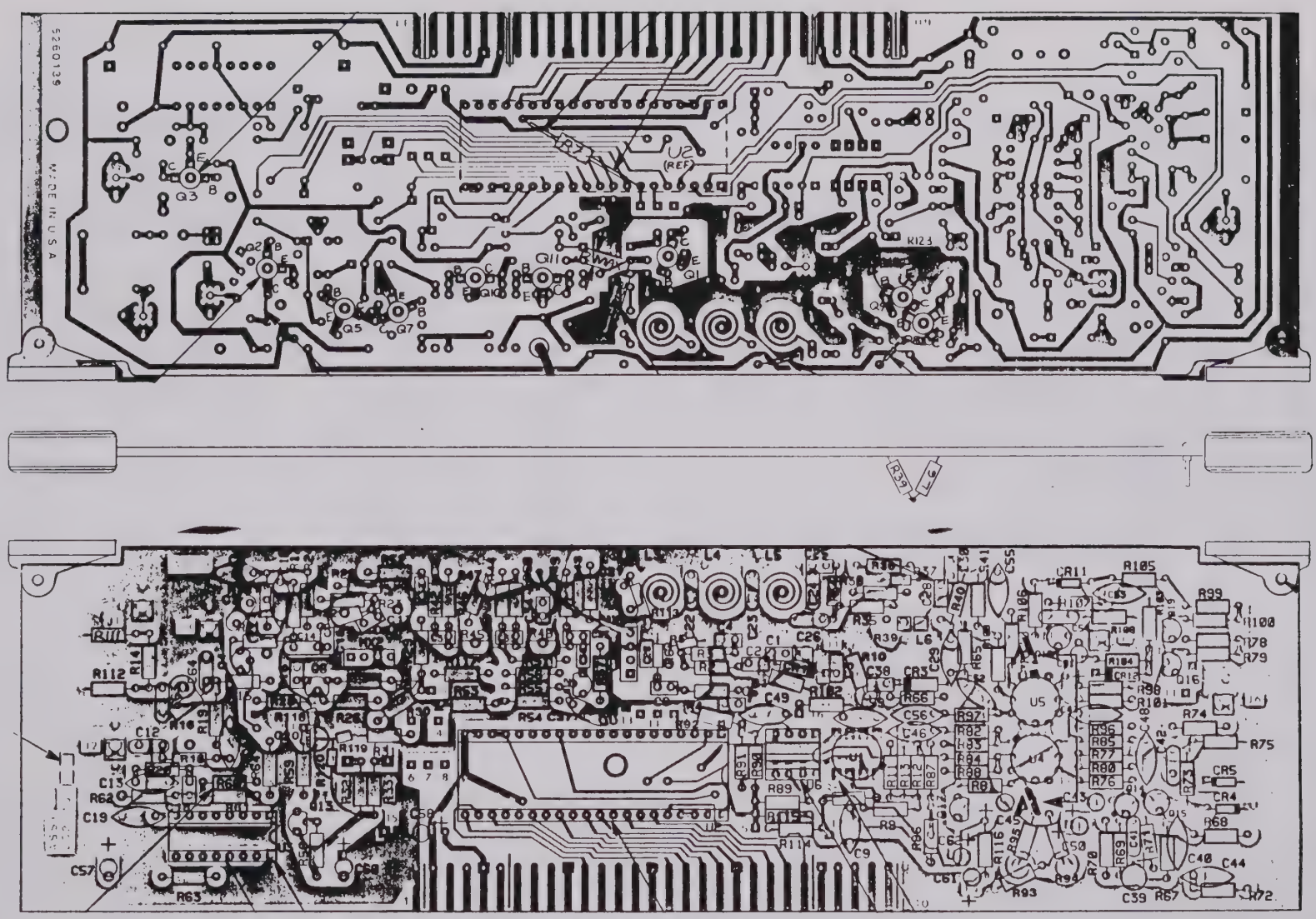
A109 BAND 2 CONVERTER (Continued) 2020139-07

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R59	R45						
R60		RES,MF	560	1/8W	1%	4130561-00	1
R61		RES,MF	82.5	1/8W	1%	4068259-00	1
R62		RES,MF	130.0	1/8W	1%	4061300-00	2
R63		RES,CC	510	1/4W	5%	4010511-00	1
R64		RES,CC	51	1/4W	5%	4010510-00	2
R65		RES,CC	200	1/4W	5%	4010201-00	1
R66		RES,CC	160K	1/4W	5%	4010164-00	1
R67		RES,M/OX	1.8K	1/4W	2%	4130182-00	1
R68	R24						
R69		RES,M/OX	510	1/4W	2%	4130511-00	2
R70		RES,M/OX SEE NOTE 6	1.2K	1/4W	2%	4130122-00	1
R71	R29						
R72	R24						
R73		RES,CC	1M	1/4W	5%	4010105-00	2
R74	R64						
R75	R73						
R76		RES,M/OX	2.2K	1/4W	2%	4130222-00	3
R77		RES,M/OX	3.9K	1/4W	2%	4130392-00	3
R78		RES,CC	5.6K	1/4W	5%	4010562-00	1
R79		RES,CC	3.6K	1/4W	5%	4010362-00	3
R80		RES,M/OX	7.5K	1/4W	2%	4130752-00	3
R81	R76						
R82	R24						
R83		RES,M/OX	200	1/4W	2%	4130201-00	3
R84	R77						
R85		RES,M/OX	330	1/4W	2%	4130331-00	1
R86		RES,CC	6.8K	1/4W	5%	4010682-00	2
R87	R79						
R88	R80						
R89	R8						
R90		RES,CC	75K	1/4W	5%	4010753-00	1
R91		RES,M/OX	33K	1/4W	2%	4130333-00	1
R92		RES,M/OX	160	1/4W	2%	4130161-00	1
R93	R21						
R94		RES,M/OX SEE NOTE 7	18	1/4W	2%	4130180-00	2
R95	R94						
R96	R83						
R97	R83						
R98	R77						
R99	R86						
R100	R79						
R101	R80						
R102	R10						
R103	R76						
R104		RES,CC	180	1/4W	5%	4010181-00	1
R105	R24						
R106		RES,MF	90.9	1/8W	1%	4069099-00	1
R107	R62						
R108	R24						
R109	R69						
R110	R17						
R111		RES,CC	160	1/4W	5%	4010161-00	2
R112	R111						
R113		RES,MF	20.0	1/8W	1%	4062009-00	1

NOTE 6 - SAT AS FOLLOWS: 820 MIN-1.6K MAX
NOTE 7 - SAT AS FOLLOWS: 12 MIN-24 MAX

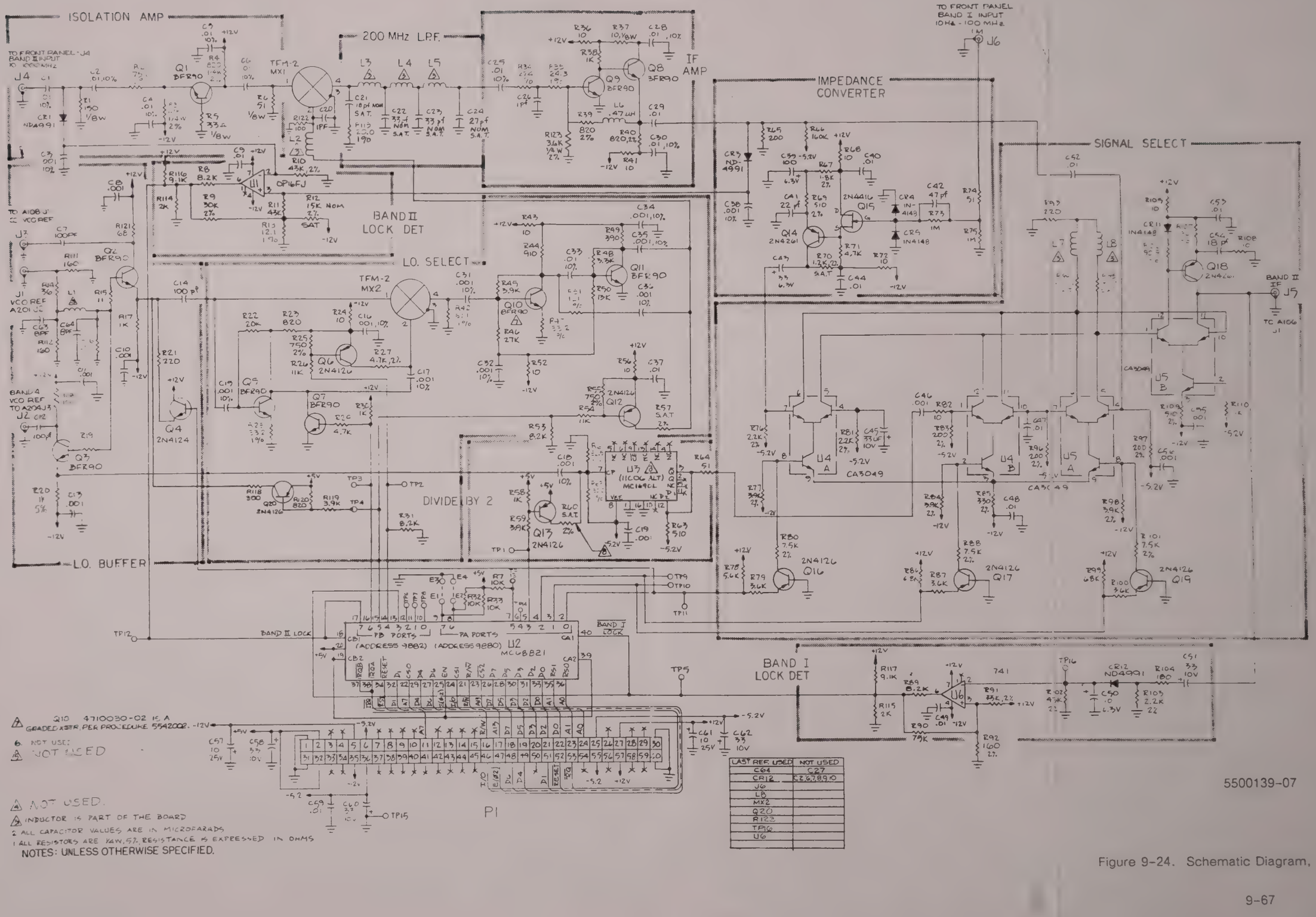
A109 BAND 2 CONVERTER (Continued) 2020139-07

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R114		RES,M/OX	2K	1/4W	2%	4130202-00	2
R115	R114						
R116		RES,M/OX	9.1K	1/4W	2%	4130912-00	2
R117	R116						
R118		RES,CC	300	1/4W	5%	4010301-00	1
R119	R45						
R120	R23						
R121		RES,CC	68	1/4W	5%	4010680-00	1
R122	R18						
R123		RES,M/OX	2.6K	1/4W	2%	4130362-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	16
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
TP6	TP1						
TP7	TP1						
TP8	TP1						
TP9	TP1						
TP10	TP1						
TP11	TP1						
TP12	TP1						
TP13	TP1						
TP14	TP1						
TP15	TP1						
TP16	TP1						
U1		IC,OP-16F,OPNL AMPL,JFET INP,TO-99				3041016-00	1
U2		IC,68B21P,PRPHL INTERFACE ADAPTER				3086821-00	1
U3		IC,11C06				3001106-00	1
U4		IC,DUAL DIFF AMPL,LIN				3043049-00	2
U5	U4						
U6		IC,LM741C,OP AMP				3040741-00	1
XU1		CONN,IC PIN(MINISERT)				2620054-00	8



8000139-02

Figure 9-23. Component Locator, Band 2 Converter



LAST REF. USED	NOT USED
C64	C27
CR12	CR6,7,8,9,10
J6	
L8	
MX2	
Q20	
R123	
TP16	
U6	

5500139-07

Figure 9-24. Schematic Diagram, Band 2 Converter

A110
FRONT PANEL
DISPLAY AND KEYBOARD
(2020140-02)

The Front Panel Display and Keyboard Assembly (A110) is divided into two functional sections.

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains twelve common anode 7-segment numeric display units (DS1-DS12), two green LED's (DS37 and DS38), and a maximum of twenty-four yellow LED's (DS13-DS36).

The twelve 7-segment LED's are mounted side by side, with space between each third digit from the right. The corresponding cathode segments of the 7-segment LED's are connected, and the drive signals come from the segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board (A111).

The twenty-four yellow LED's (DS13-DS36) are divided into three groups of 8 LED's each. The anodes of all LED's in each group are connected. The cathode of each LED in a group are connected to one of the segment drivers (Q3-Q10). With this arrangement each group of annunciator lights can be regarded as similar to one 7-segment LED. The digit drives for the 3 groups of annunciator lights also come from the Front Panel Logic board (A111).

The two green LED's (DS37 and DS38) are driven by Q1 and Q2. When these LED's light they indicate that GATE and CONVERTER SEARCH are in operation.

KEYBOARD

This section of the assembly makes provision for a maximum of twenty-five (single-pole double-throw) switches of which only 21 are used. The switches are arranged in a 4 row by 6 column matrix, with the extra switch taking the row 4 column 7 position. The columns are connected to +5V through the resistor network (RN1) on the Front Panel Logic board (A111).

The keyboard is continuously scanned. The signals scanning the keyboard are derived from A111. To scan the keyboard the 4 rows are grounded sequentially. When a row is grounded, and a key in that row is pushed, one of the columns will be grounded. This information is sent to the A111 board where key debouncing is performed.

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A110 FRONT PANEL DISPLAY AND KEYBOARD 2020140-02

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
DS1		LAMP,LED,NUMERIC INDICATOR				2800024-01	12
DS2	DS1						
DS3	DS1						
DS4	DS1						
DS5	DS1						
DS6	DS1						
DS7	DS1						
DS8	DS1						
DS9	DS1						
DS10	DS1						
DS11	DS1						
DS12	DS1						
DS13		LAMP,LED,YELLOW,RECT .15X.25				2800020-00	24
DS14	DS13						
DS15	DS13						
DS16	DS13						
DS17	DS13						
DS18	DS13						
DS19	DS13						
DS20	DS13						
DS21	DS13						
DS22	DS13						
DS23	DS13						
DS24	DS13						
DS25	DS13						
DS26	DS13						
DS27	DS13						
DS28	DS13						
DS29	DS13						
DS30	DS13						
DS31	DS13						
DS32	DS13						
DS33	DS13						
DS34	DS13						
DS35	DS13						
DS36	DS13						
DS37		LAMP,LED,GREEN,.12 OD				2800018-00	2
DS38	DS37						
P1		CONN,PCB RCPT,9 PIN				2620065-00	1
P2		CONN,PCB RCPT,17 PIN				2620067-00	1
P3		CONN,PCB RCPT,13 PIN				2620066-00	1
Q1		XSTR,2N4402,PNP,RF AMPLIFIER				4710019-00	10
Q2	Q1						
Q3	Q1						
Q4	Q1						
Q5	Q1						
Q6	Q1						
Q7	Q1						
Q8	Q1						
Q9	Q1						
Q10	Q1						
R1		RES,CC	4.7K	1/4W	5%	4010472-00	2
R2		RES,CC	130	1/4W	5%	4010131-00	2
R3	R1						
R4	R2						
R5		RES,CC	240	1/4W	5%	4010241-00	8
R6		RES,CC	18	1/4W	5%	4010180-00	8
R7	R5						
R8	R6						

A110 FRONT PANEL DISPLAY AND KEYBOARD (Continued) 2020140-02

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
R9	R5			
R10	R6			
R11	R5			
R12	R6			
R13	R5			
R14	R6			
R15	R5			
R16	R6			
R17	R5			
R18	R6			
R19	R5			
R20	R6			
S1		SWITCH,MOM SPDT	4500013-00	21
S2		NOT USED		
S3		NOT USED		
S4		NOT USED		
S5		NOT USED		
S6	S1			
S7	S1			
S8	S1			
S9	S1			
S10	S1			
S11	S1			
S12	S1			
S13	S1			
S14	S1			
S15	S1			
S16	S1			
S17	S1			
S18	S1			
S19	S1			
S20	S1			
S21	S1			
S22	S1			
S23	S1			
S24	S1			
S25	S1			
XDS1		CONN,SOCKET,DIP,14 PIN	2630015-00	12
XDS2	XDS1			
XDS3	XDS1			
XDS4	XDS1			
XDS5	XDS1			
XDS6	XDS1			
XDS7	XDS1			
XDS8	XDS1			
XDS9	XDS1			
XDS10	XDS1			
XDS11	XDS1			
XDS12	XDS1			
XDS13		CONN,IC PIN (MINISERT)	2620054-00	48
XDS14	XDS13			
XDS15	XDS13			
XDS16	XDS13			
XDS17	XDS13			
XDS18	XDS13			

A110 FRONT PANEL DISPLAY AND KEYBOARD (Continued) 2020140-02

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
XDS19	XDS13			
XDS20	XDS13			
XDS21	XDS13			
XDS22	XDS13			
XDS23	XDS13			
XDS24	XDS13			
XDS25	XDS13			
XDS26	XDS13			
XDS27	XDS13			
XDS28	XDS13			
XDS29	XDS13			
XDS30	XDS13			
XDS31	XDS13			
XDS32	XDS13			
XDS33	XDS13			
XDS34	XDS13			
XDS35	XDS13			
XDS36	XDS13			

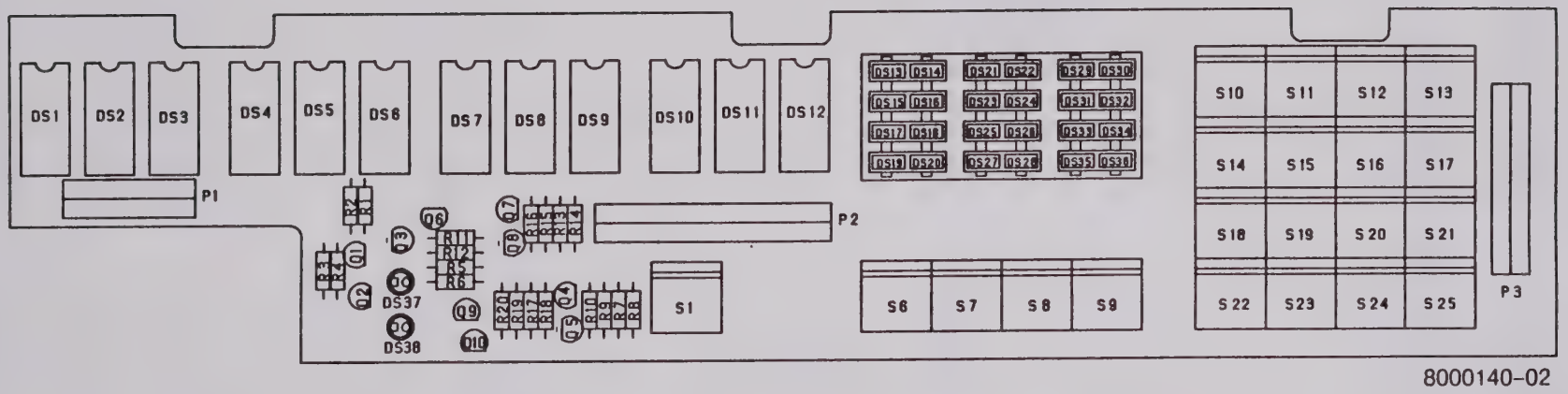
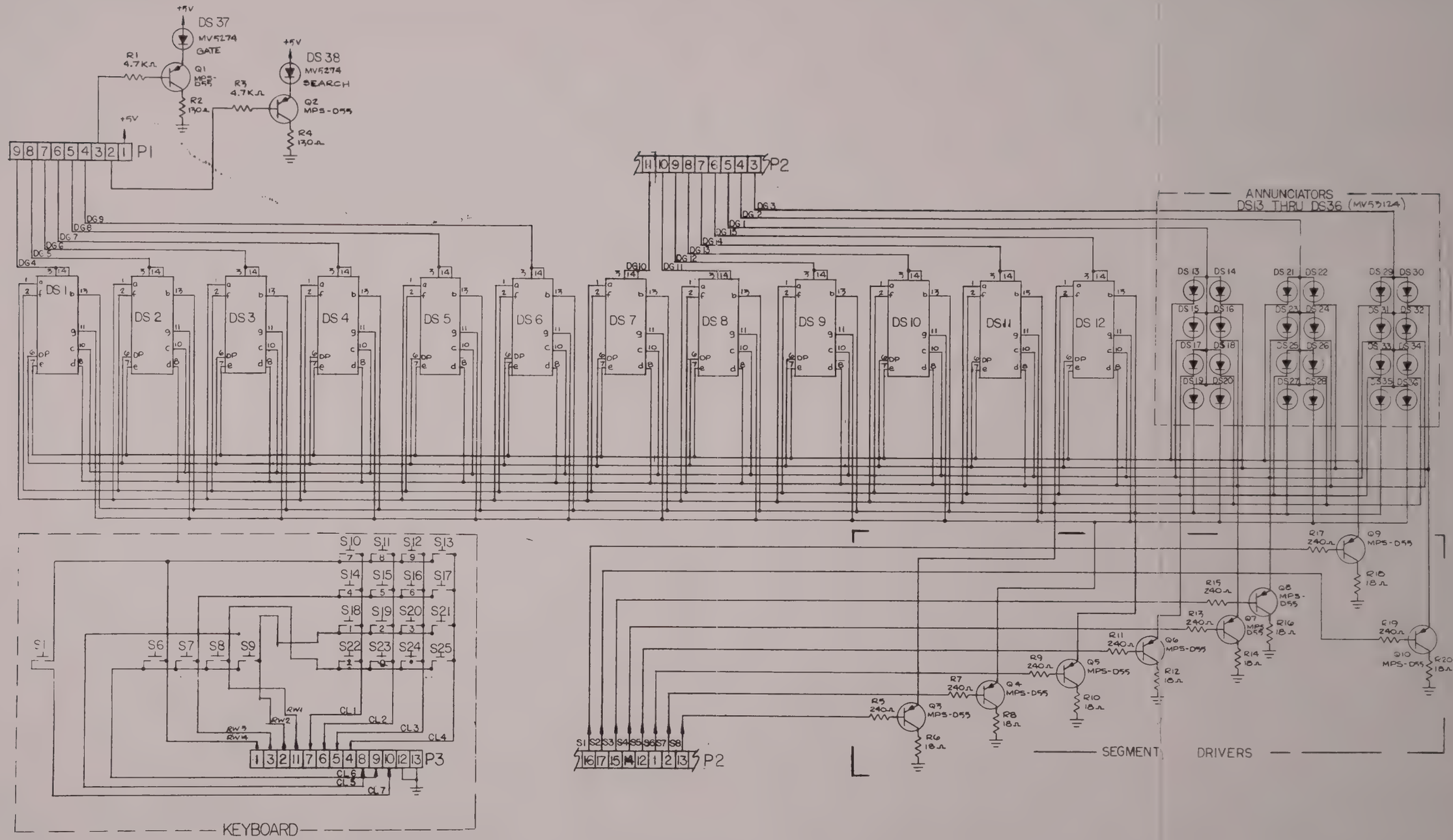


Figure 9-25. Component Locator, Front Panel Display and Keyboard



2. ALL CAPACITOR VALUES ARE EXPRESSED IN MICROFARADS.
1. ALL RESISTORS ARE ¼ W, ± 5%. RESISTANCE IS EXPRESSED IN OHMS.
NOTES: UNLESS OTHERWISE SPECIFIED.

5500140-00

Figure 9-26. Schematic Diagram, Front Panel Display and Keyboard

A111
FRONT PANEL LOGIC
(2020191-02)

The Front Panel Logic Assembly (A111) contains logic circuitry for control of two functions.

- Display Control
- Keyboard Control

The +5 V power supply to the front panel assemblies (A110 and A111) is regulated by a voltage regulator that is located behind the A111 board. For heatsinking purposes, this voltage regulator is mounted on the chassis. Please refer to Figure 9-28, Front Panel Logic Block Diagram on page 9-79.

DISPLAY CONTROL

The twelve 7-segment LEDs and the three groups of annunciator lights on A110 are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by 4 to 16 line multiplexer (U2), and the appropriate digit driver is turned on. At this time the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit), turns the segment drivers (A110) on or off.

The display intensity is controlled by varying the duty cycle of the multiplexing. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation the GATE light control is triggered, and the GATE LED lights for the length of the GATE.

MEMORY UPDATE MODE

In this mode the multiplexer logic is disabled by setting the display scan/$\overline{\text{update}}$ control line (PA4) to logic 0. The microprocessor controlled clock ($\overline{\text{clock}}$, PA1) is used to clock the display counter (U6).

Before updating the display memory (U7 and U8), the display counter is cleared by setting the clear/load control line (PA5) to logic 1, and clocking the clock input of U6. Update mode timing is illustrated in Figure 9-27.

KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the keyboard READ/$\overline{\text{SCAN}}$ control line (PA0) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pushed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. When a key is pushed, the column containing that key will be grounded. The output of U13 goes to logic 1 and C7 (in the debounce circuit) starts to discharge. When the voltage across C7 reaches approximately +0.7 V above ground, the debounce circuit will trigger the interrupt input on the PIA (U11, pin 18) indicating that a key is being pushed.

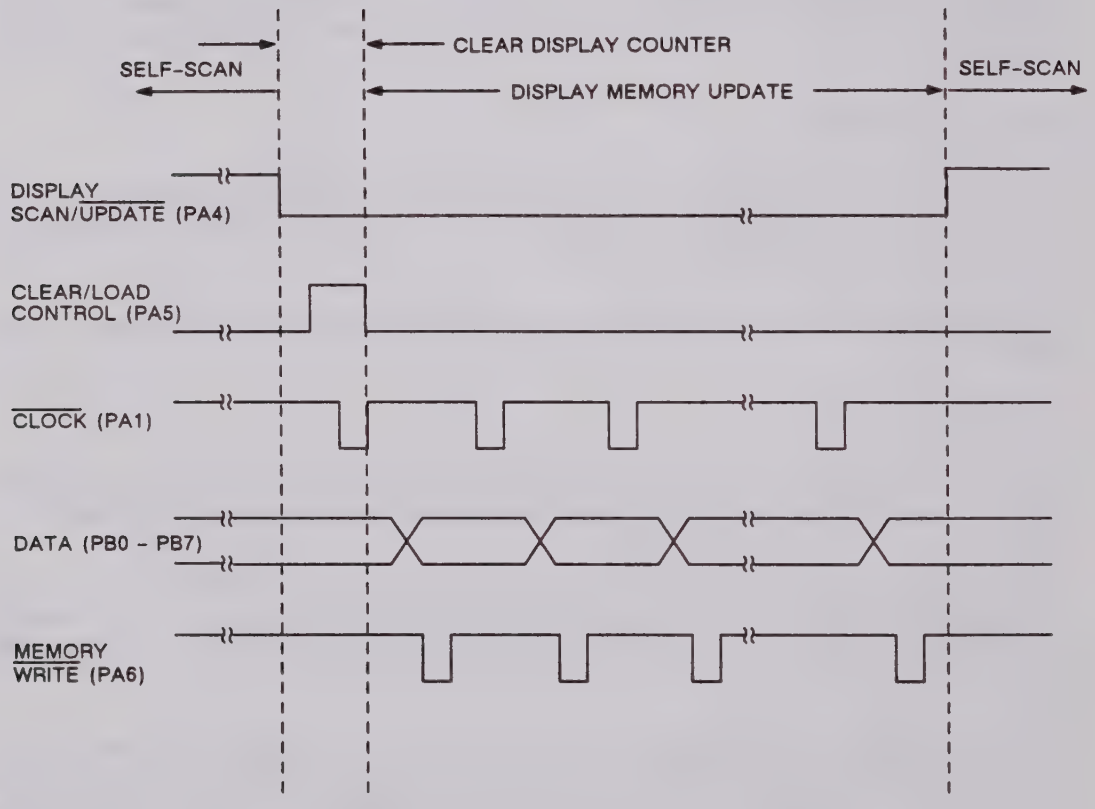


Figure 9-27. Memory Update Mode Sequence

READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 is put on the keyboard READ/$\overline{\text{SCAN}}$ control line (PA0). This enables the data buffer (U9). A 0111 is then loaded into the shift register (U3) by putting a logic 1 on the CLEAR/LOAD control line (PA5) and clocking the clock input of U3. The logic 0 at the output of the shift register (U3) is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the 4 outputs of U3 to determine the coordinate of the key pushed. After the keyboard is read, the keyboard READ/$\overline{\text{SCAN}}$ line is returned to logic 0.

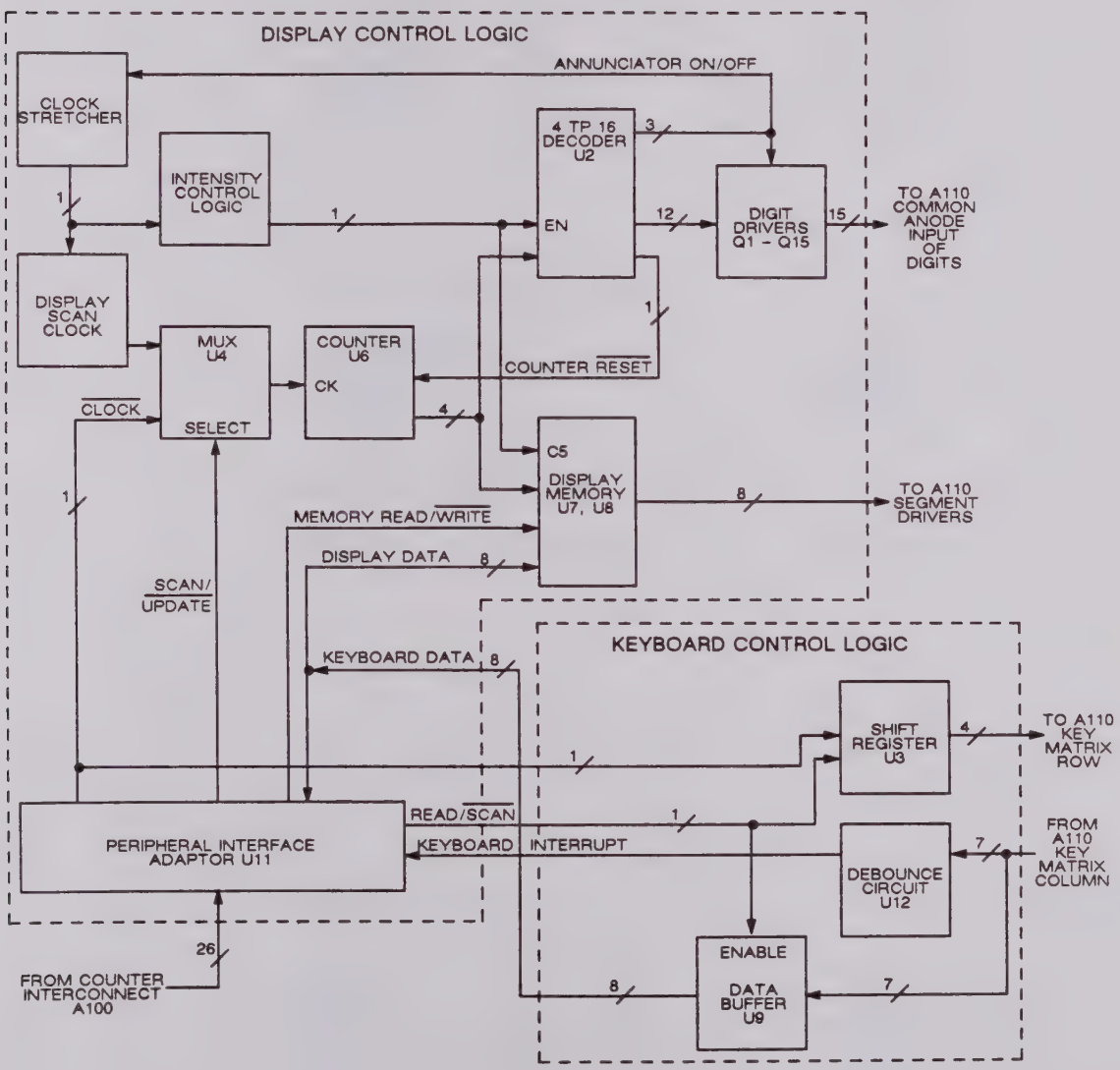


Figure 9-28. Front Panel Logic Block Diagram

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A111 FRONT PANEL LOGIC 2020191-02

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,TANTALUM	.1µF		35V	2300020-00	1
C2		CAP,DISC,CER	.002µF	20%	1KV	2150005-00	2
C3	C2						
C4		NOT USED					
C5		CAP,TANTALUM	47µF		16V	2300025-00	1
C6		CAP,TANTALUM	2.2µF	20%	16V	2300012-00	1
C7		CAP,TANTALUM	22µF	20%	16V	2300030-00	1
C8		CAP,TANTALUM	.33µF	20%	35V	2300031-00	1
C9		CAP,TANTALUM	33µF		10V	2300015-00	1
C10		CAP,CER	.01µF	20%	100V	2150003-00	6
C11	C10						
C12	C10						
C13	C10						
C14	C10						
C15	C10						
CR1		DIODE,1N4148,FAST SWITCHING,GP				2704148-00	1
J1		CONN,PCB,PLUG,9 PIN				2620062-00	1
J2		CONN,PCB,PLUG,17 PIN				2620064-00	1
J3		CONN,PCB,PLUG,13 PIN				2620063-00	1
J4		CONN,FRICT LK .100,4 PIN				2620068-00	1
J5		CONN,FRICT LK .100,3 PIN				2620121-00	1
P1		NOT USED					
P2		CONN,PCB,RT ANGLE,26 PIN				2620131-00	1
Q1		XSTR,MPSD54,PNP,DARLINGTON				4710027-00	15
Q2	Q1						
Q3	Q1						
Q4	Q1						
Q5	Q1						
Q6	Q1						
Q7	Q1						
Q8	Q1						
Q9	Q1						
Q10	Q1						
Q11	Q1						
Q12	Q1						
Q13	Q1						
Q14	Q1						
Q15	Q1						
Q16		XSTR,2N4124,NPN,GP				4704124-00	2
Q17	Q16						
R1		RES,CC	10K	1/4W	5%	4010103-00	2
R2		RES,CC	220	1/4W	5%	4010221-00	1
R3		RES,CC	75K	1/4W	5%	4010753-00	1
R4		POT,CERMET	200	KT05	0.5W	4250022-00	1
R5		RES,CC	120K	1/4W	5%	4010124-00	1
R6		RES,CC	2.4K	1/4W	5%	4010242-00	1
R7		RES,CC	1K	1/4W	5%	4010102-00	16
R8	R7						
R9	R7						
R10	R7						
R11	R7						
R12	R7						
R13	R7						
R14	R7						
R15	R7						

A111 FRONT PANEL LOGIC (Continued) 2020191-02

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R16	R7						
R17	R7						
R18	R7						
R19	R7						
R20	R7						
R21	R7						
R22		NOT USED					
R23		RES,CC	15K	1/4W	5%	4010153-00	1
R24		RES,CC	390	1/4W	5%	4010391-00	1
R25		RES,CC	200	1/4W	5%	4010201-00	1
R26	R7	SEE NOTE 1					
R27	R1						
R28		NOT USED					
R29		RES,CC	2.2K	1/4W	5%	4010222-00	1
R30		NOT USED					
R31		RES,CC	27K	1/4W	5%	4010273-00	1
R32		RES,CC	39K	1/4W	5%	4010393-00	3
R33	R32						
R34	R32						
RN1		RES,NTWK	9X10K	0.2W	2%	4170003-00	2
RN2	RN1						
RN3		RES,NTWK	7X10K	0.3W	2%	4170004-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	9
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
TP6	TP1						
TP7		NOT USED					
TP8	TP1						
TP9	TP1						
TP10	TP1						
U1		IC,74LS123				3084123-00	2
U2		IC,74154				3074154-00	1
U3		IC,SR,PRL ACCESS,4-BIT,TI ONLY				3084195-01	1
U4		IC,74LS51				3087451-00	1
U5		IC,74LS132				3084132-00	1
U6		IC,74LS163				3084163-00	1
U7		IC,74LS189				3057489-00	2
U8	U7						
U9		IC,74LS244				3084244-00	1
U10	U1						
U11		IC,68B21P,PRPHL INTERFACE ADAPTER				3086821-00	1
U12		IC,74LS14				3087414-00	1
U13		IC,74LS30				3987430-00	1

NOTE 1 - R26 SAT AS FOLLOWS: 820 OHMS MIN-1.2K OHMS MAX

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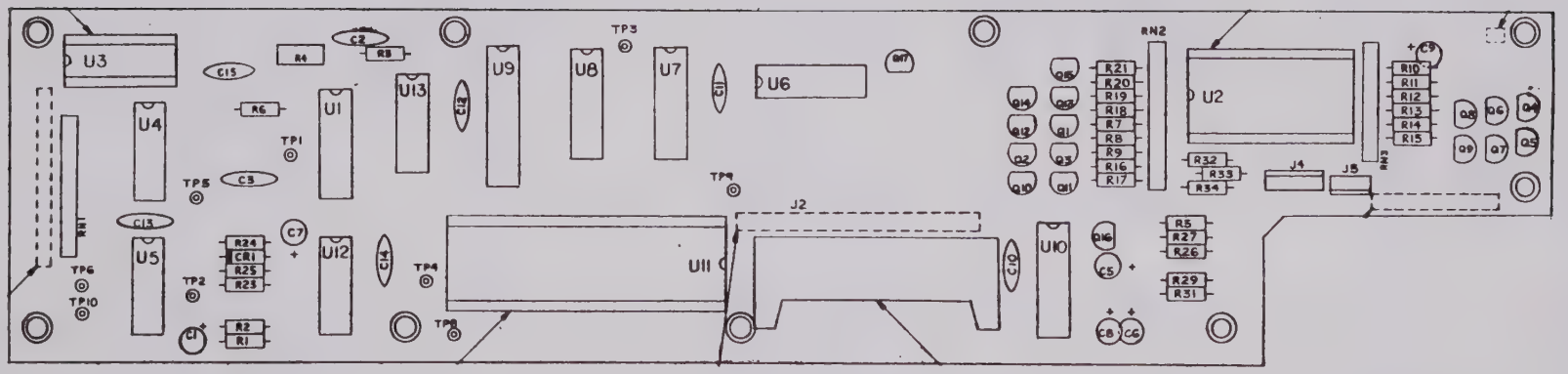

8000191-01

Figure 9-29. Component Locator, Front Panel Logic

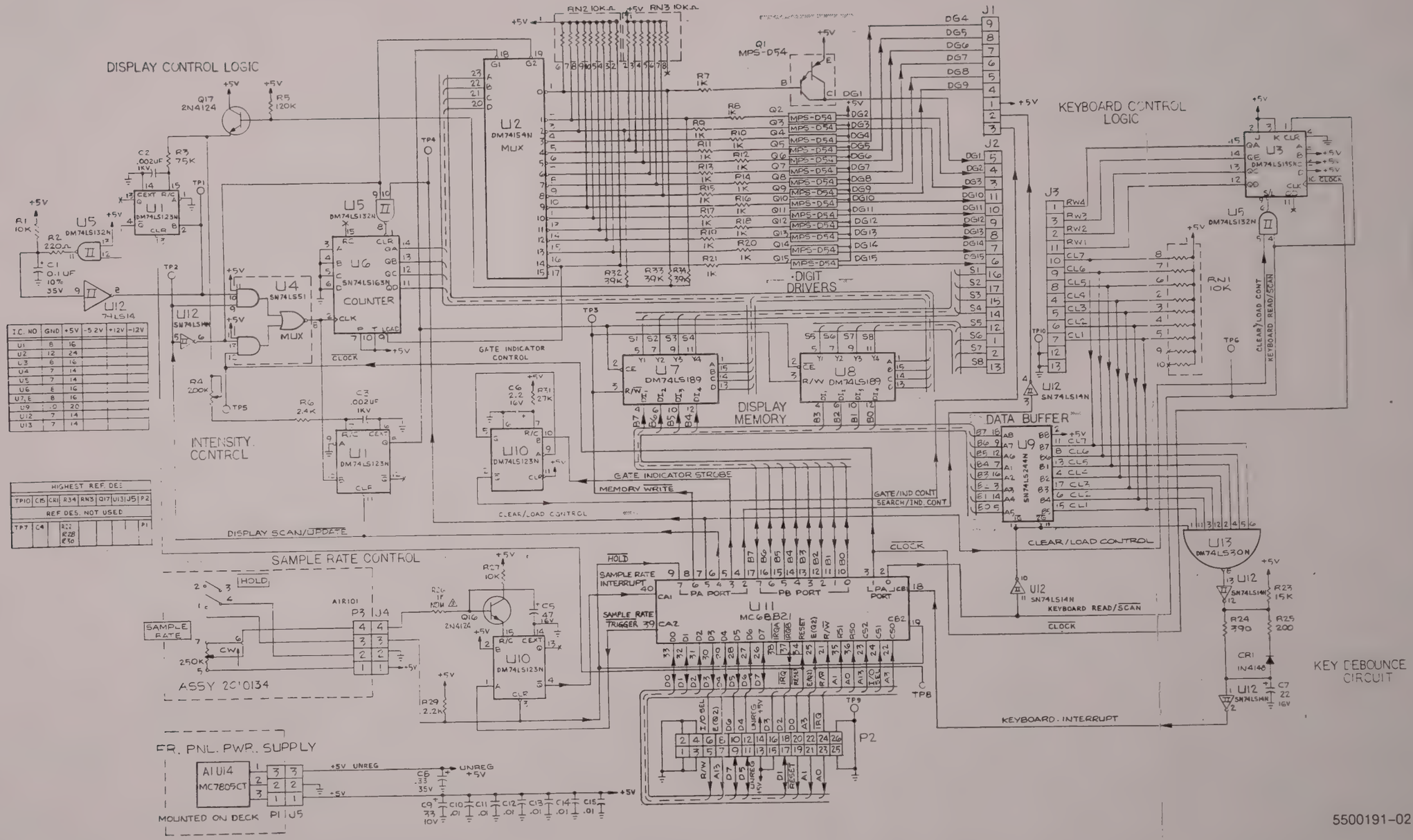

Figure 9-30. Schematic Diagram, Front Panel Logic

A203
BAND 3 MICROWAVE CONVERTER

The A203 Microwave Converter consists of three functional sections:

- Voltage Control Oscillator (A201A)
- IF Amplifier (A201B)
- Microwave (YIG) (A202)

CAUTION

Disassembly of the A202 Microwave Assembly, or removal of it from the A201A VCO or A201B IF Amplifier will void the EIP warranty.

The assembly drawing and schematic for both the VCO and IF circuits are not available. The entire A203 assembly must be tested as a complete unit to ensure proper performance of the counter. Repair of the Microwave (YIG) module can only be done at the factory. The VCO and IF Amplifier boards require special test equipment, therefore field repair is not recommended.

The Band 3 Converter is a complete microwave subsystem (see Figure 9-31) which converts an input signal in the 1 to 20 (26.5) GHz range down to an IF of 127 MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal (FVCO). The mixer then produces a signal (FIF) equal to the difference between the input and reference harmonic. If this difference is close to 127 MHz, it is amplified to a level of about 0 dBm and then counted. The input signal is then determined from the equation FIN = NFVCO + FIF. FVCO is set by the instrument program via a phase locked loop located on the converter control board (A108) and is thus known exactly. Harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to approximately determine the input frequency and from this information the desired values of N, FVCO and ± are determined.

Two other outputs are obtained from the Band 3 Converter. The first is an analog signal which is a measure of input RF power. The second is a digital signal ($\overline{\text{IF THRESHOLD}}$) which indicates that an IF signal exists at a level of -3 dBm or greater.

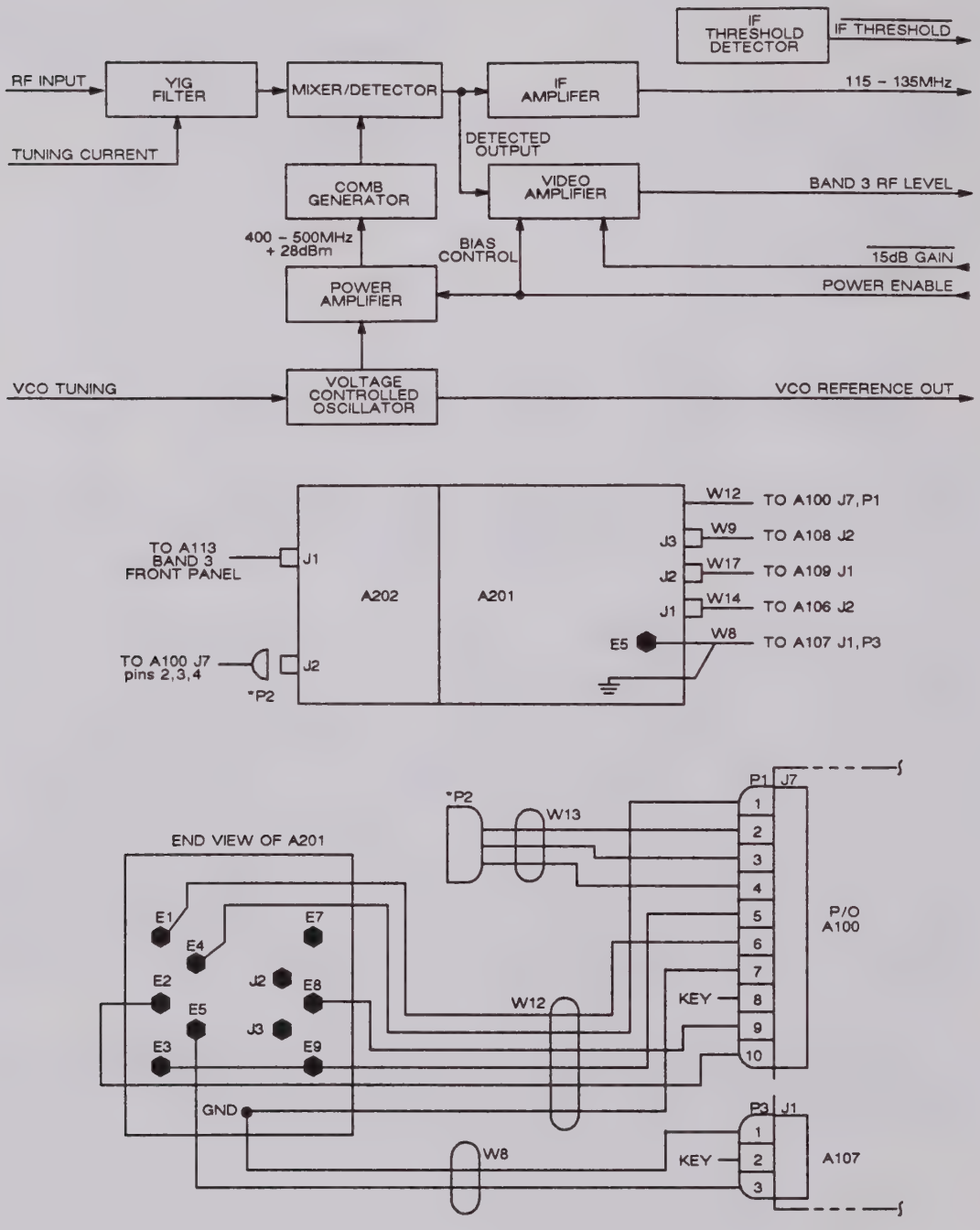

Figure 9-31. Band 3 Microwave Converter Diagram

Section 10
Options

Section 10 provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model 545B or 548B counter.

OPTION

01 D TO A CONVERTER

DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER MEASUREMENT

1 to 20/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.

Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

03 TIME BASE OSCILLATOR $<5 \times 10^{-9}$ (2010143-03)

04 TIME BASE OSCILLATOR $<1 \times 10^{-9}$ (2010143-04)

05 TIME BASE OSCILLATOR $<5 \times 10^{-10}$ (2010143-05)

06 EXTENDED FREQUENCY CAPABILITY - 548B

Use in conjunction with model 590 Frequency Extension Cable Kit and optional Remote Sensors models 91 thru 98.

07 NOT USED

08 GENERAL PURPOSE INTERFACE BUS (GPIB)

09 REAR PANEL INPUT

10 CHASSIS SLIDES

OPTION 01
DIGITAL TO ANALOG CONVERTER

Option 01 will convert three consecutive digits to an analog voltage, available on the rear panel. The output will reflect the display, substituting zeros for any non-numeric characters that appear. The output will be updated after every display update.

SPECIFICATIONS

Output Voltage	0.000 volts to 0.999 volts
Accuracy (2° C)	± 0.5 % ± 1 mV
Temp. Stability (0-50° C)	± 0.01 % / ° C
Resolution	1 mV
Load Impedance	1 K ohm minimum
Connector	BNC female (on rear panel)
Protection	±10 V AC or DC applied to output connector will not cause damage. No damage will occur by any load.

OPERATION

On power up, the DAC is in off state.

KEYBOARD OPERATION

A three key sequence slects the location of the most significant digit in the three digits desired. Digits are numbered 01 through 12.

PRESS: DAC [ ] [x] [x] XX can vary from 01 to 12.

Examples:

DAC [ ] [0] [1] 1 Hz digit selected

DAC [ ] [0] [2] 10 Hz, 1 Hz digits selected

DAC [ ] [0] [3] 100 Hz, 10 Hz, 1 Hz digits

DAC [ ] [0] [4] 1 kHz, 100 Hz, 10 Hz digits

•
•
•

DAC [ ] [1] [2] 100 GHz, 10 GHz, 1 GHz digits

After pressing DAC [ ], the display will show the present DAC status, such as DAC OFF or DAC XX. Three decimal points will show the locations of the currently selected digits (if DAC is on).

After pressing the first [×], the display will show the temporary entry, e.g., DAC X, but the three decimal points will still show the previous DAC status.

After pressing the second [×], the display will show the new entry, e.g., DAC X X. The three decimal points will move to the newly selected locations. The DAC output will be updated accordingly. Release of the last key pressed will return the display to display measurements.

Any illegal key stroked will result in displaying ERROR 10. The operator must restart the key sequence to enter the correct data.

To clear display of DAC data, ERROR display, or an unfinished key sequence, press [CLEAR DISPLAY]. Display to return to display measurements, and DAC status will not be changed.

To turn off DAC option Press: [DAC] [DATA CLEAR] OR [DAC] [0] [0]

REMOTE OPERATION

For remote operation through GPIB, refer to the GPIB (Option 08) section of this manual.

THEORY OF OPERATION

A simplified block diagram of the DAC portion of the A103 board is shown in Figure 10–1.

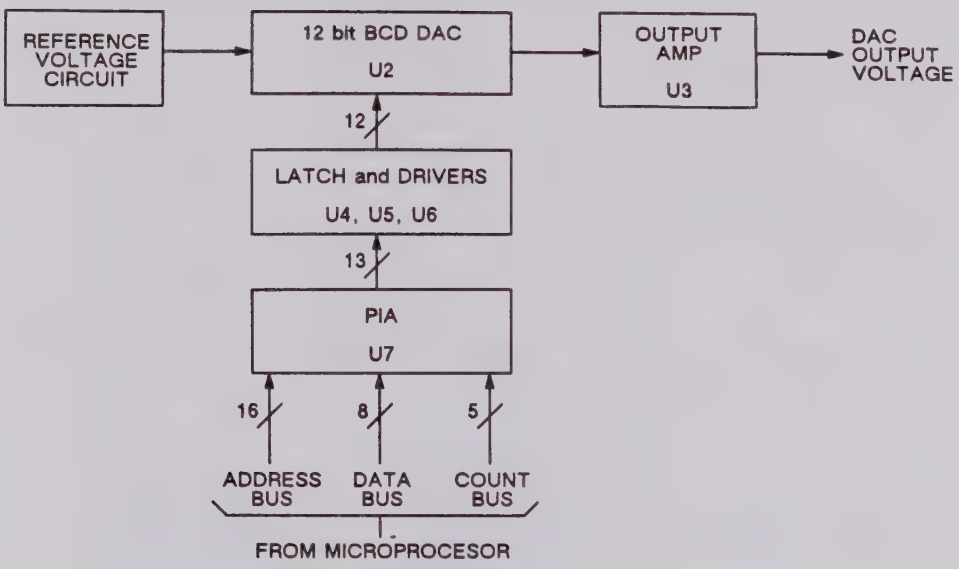

Figure 10–1. DAC Option, Simplified

HARDWARE

PIA AND LATCH DRIVER BLOCKS

The 3 selected digits are manipulated by the program and sent to the PIA. First the 2 LSD's are sent to port A, then the third digit (MSD) plus a positive-going pulse (on pin 14 of U7) that triggers the latch U6 so that the complete 12 bit word appears to the DAC inputs (U2). U4 and U5 are level translators from T^2L to CMOS for the DAC.

ANALOG BLOCKS

The DAC is referenced to a 1 volt reference voltage that is generated by CR1 zener and U1 Operational Amplifier. Gain adjustment is provided to calibrate the reference voltage. The DAC U2 converts the 12 bit digital inputs to an analog voltage (0.000V – 0.999V). The output amplifier U3 provides the necessary I/V conversion, output isolation and protection. Zero offset adjustment is provided for calibration purposes, also.

SOFTWARE

The DAC software is described in Figures 10–2 and 10–3.

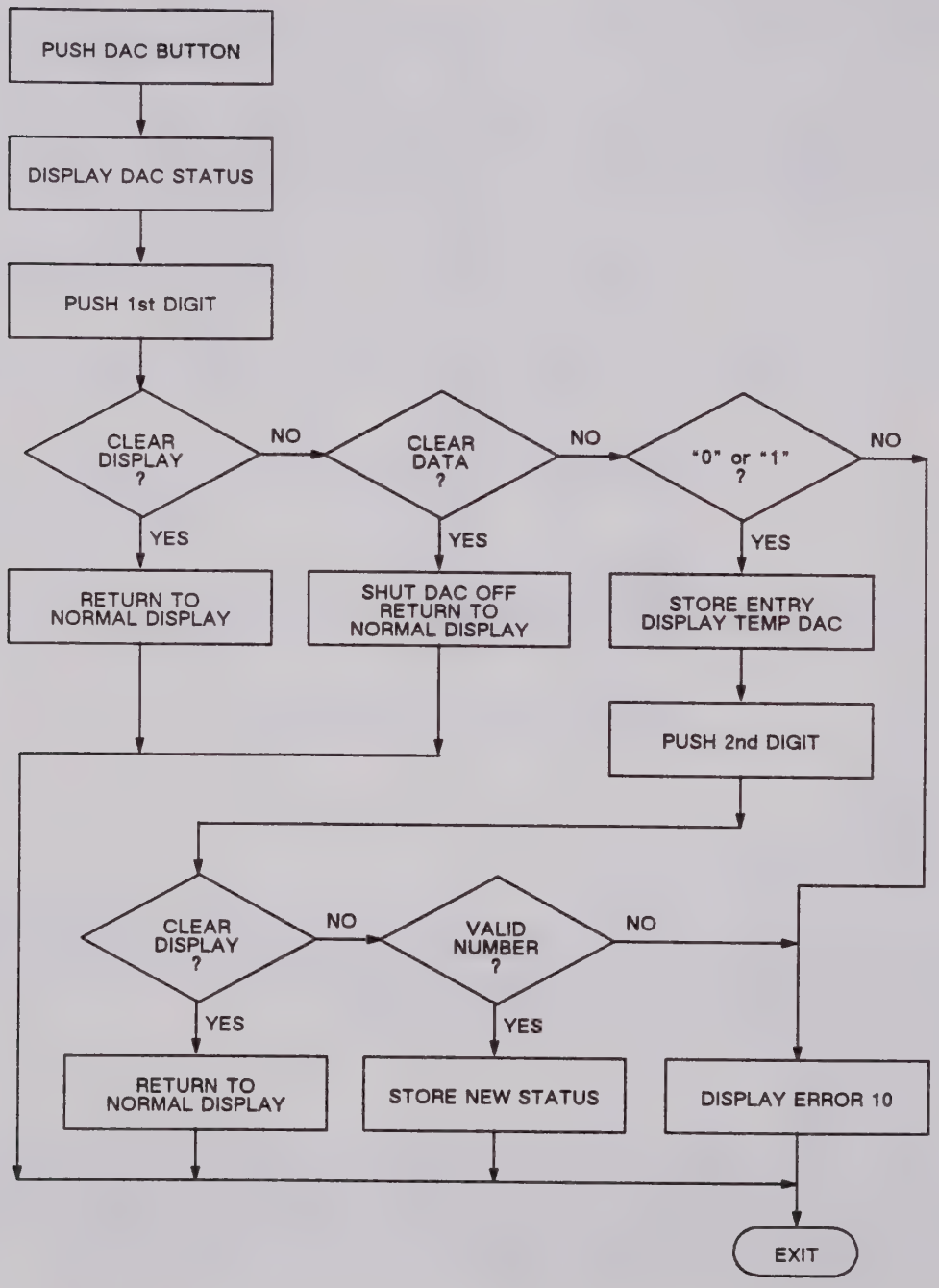

Figure 10-2. Keyboard Control

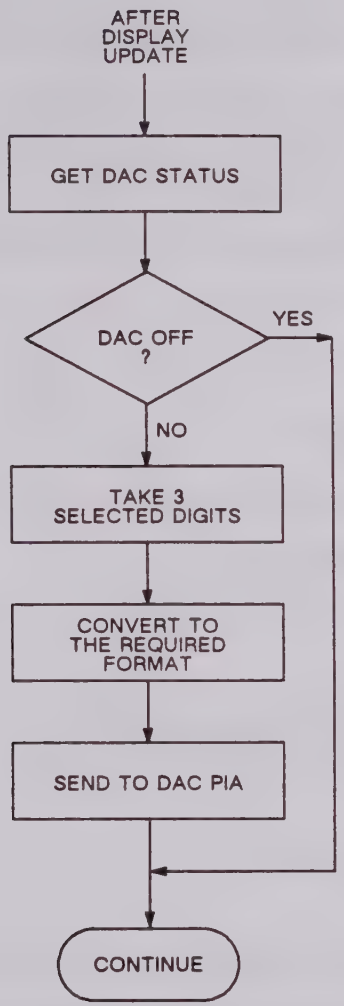

Figure 10-3. DAC Board Update

CALIBRATION

The following instruments or their equivalents are required to perform calibration of the DAC board. Calibration is required every six months or after the board has been repaired.

BRAND	MODEL	TYPE	SPECIFICATIONS
Fluke	8050A	DVM	4 1/2 digit resolution

ZERO OFFSET CALIBRATION

1. Turn on the counter with no input, so that the display shows all zeros.
2. Enter: DAC [ ] [0] [3]
3. Connect digital volt meter to the rear DAC output.
4. Adjust R6 to reach 0.000 volts on the DVM display.

FULL SCALE CALIBRATION

1. Short TP3 to TP4.
2. Adjust R4 to reach 1.000 volts on the DVM display.
3. Remove the short.

The calibration for the DAC board is complete.

PERFORMANCE TESTS

Refer to the instruments table in Calibration for the required test equipment.

Connect the DVM and the DAC output (rear panel). Connect rear 10 MHz output to Band 1 input.

PRESS: BAND [ ] [1] RESOL [ ] [2] Display shows 10.000 0 MHz.

ACCURACY TEST

PRESS: DAC [ ] [0] [6] DVM should read 0 ±1mV.

PRESS: FREQ OFFSET [ ] [•] [9] [9] [9] MHz [ ] DVM should read 0.999 ±0.006 V.

Repeat the second test in accuracy for entries between .888 and .111. DVM should read the entry ±1 mV ±0.5% of entry.

TROUBLESHOOTING

1. If zero offset calibration cannot be achieved, check that all digital inputs to U2 (pins 3 to 15) are at "low" levels (+0.5V). If they are not, replace U2 or U3.

2. If full scale calibration cannot be achieved, check that voltage at TP1 is 6.2V. If voltage is wrong, replace CR1 or R1 after verifying the +12V supply. If the voltage at TP1 is 6.2V, check TP2. The voltage at TP2 should be 1.000V. If it is not, the failure is in U1 or the resistors R2, R3, or R4. If TP2 voltage is still not 1.000V, replace U2.

3. The digital lines in the DAC board can be checked in three ways.

   - With a static test implemented by connecting the rear time base 10 MHz output to Band 1 input.

     PRESS: [BAND] [1] [RESOL] [2] Display shows 10.000 0 MHz.

     PRESS: [DAC] [0] [6]

     Now entering [FREQ/OFFSET] [•] [X] [X] [X] [MHz] will cause a display of 10.XXX0 MHz.

     The XXX are selected to the DAC board, so the three BCD's should appear on U7, pins 2 to 13 (pin 2 is the LSB). On pin 14 there should be positive pulses. Checking two combinations like 777 and 888 can locate a fault in the digital path between U7 outputs and U2 inputs.

   - A dynamic test that is provided with the DAC option.

     PRESS: [TEST] [1] [1]

     A continuous count ramp from 000 to 999 is sent to the DAC board, regardless of DAC status or display.

     Connect the DAC rear output to an oscilloscope. A ramp should be observed going from 0 to .999 volts. The ramp is built with 1 mV amplitude steps. Any failure in one or more digital lines in the board will cause either breaking in the ramp or a multiple amplitude steps (2mV, 4mV, etc.). Careful analysis will show the bad line or lines.

   - Signature analysis while operating in the dynamic test just described, and checking the following signatures.

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OPTION 01 – DIGITAL TO ANALOG CONVERTER 2020145-03

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,CER	.01mF	20%	100V	2150003-00	6
C2	C1						
C3		CAP,MICA	100PF	5%	500V	2260034-00	1
C4	C1						
C5	C1						
C6		CAP,TANTALUM	33mF		10V	2300015-00	3
C7	C1						
C8	C1						
C9	C6						
C10		CAP,TANTALUM	10mF	20%	25V	2300029-00	2
C11	C10						
C12	C6						
CR1		DIODE,1N827,ZENER,6.2V				2700827-00	1
CR2		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	1
J1		CONN,COAX PC RCPT,SNAP NANOHEX				2610038-00	1
R1		RES,CC	750	1/4W	5%	4010751-00	1
R2		RES,MF	20K	1/10W	1%	4052002-00	1
R3		RES,MF PRON	2.87K	1/8W	1%	4062871-00	1
R4		POT,WW	500		10%	4280009-00	1
R5		RES,CC	10K	1/4W	5%	4010103-00	1
R6		POT,WW	10K		10%	4280006-00	1
R7		RES,CC	1K	1/4W	5%	4010102-00	1
RN1		RES,NTWK	7X10K	0.3W	2%	4170004-00	2
RN2	RN1						
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	5
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
U1		IC,LM741C,OP AMP				3040741-00	1
U2		IC,AD7525K,POT,DIGITALLY CONTROLLED				3050752-00	1
U3		IC,OP-16F,OPNL AMPL,JFET INP,TO-99				3041016-00	1
U4		IC,7407				3007407-00	2
U5	U4						
U6		IC,74C373,8-BIT LATCH				3034373-00	1
U7		IC,68B210,PRPHL INTERFACE ADAPTER				3086821-00	1
XU1		CONN,SOCKET,DIP,8 PIN				2630014-00	1
XU2		CONN,SOCKET,DIP,18 PIN				2630017-00	1
XU3		CONN,SOCKET,HOLLOW PIN				2630008-00	7
XU4		CONN,SOCKET,DIP,17 PIN				2630015-00	2
XU5	XU4						
XU6		CONN,SOCKET,DIP,20 PIN				2630018-00	1
XU7		CONN,SOCKET,DIP,40 PIN				2630022-00	1

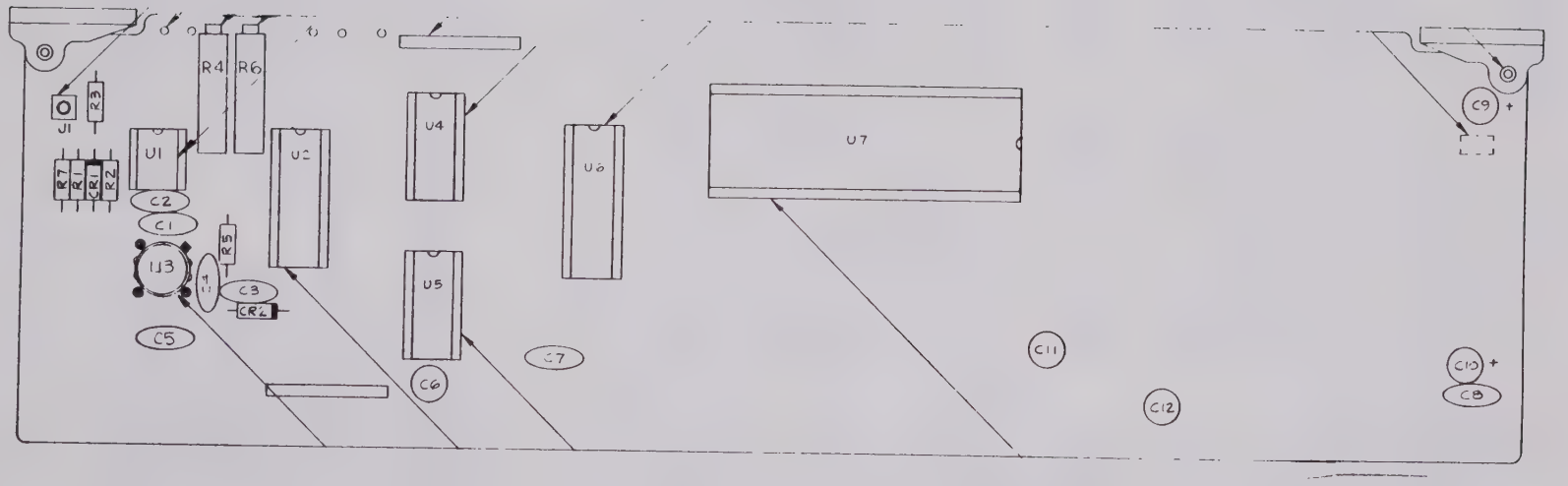
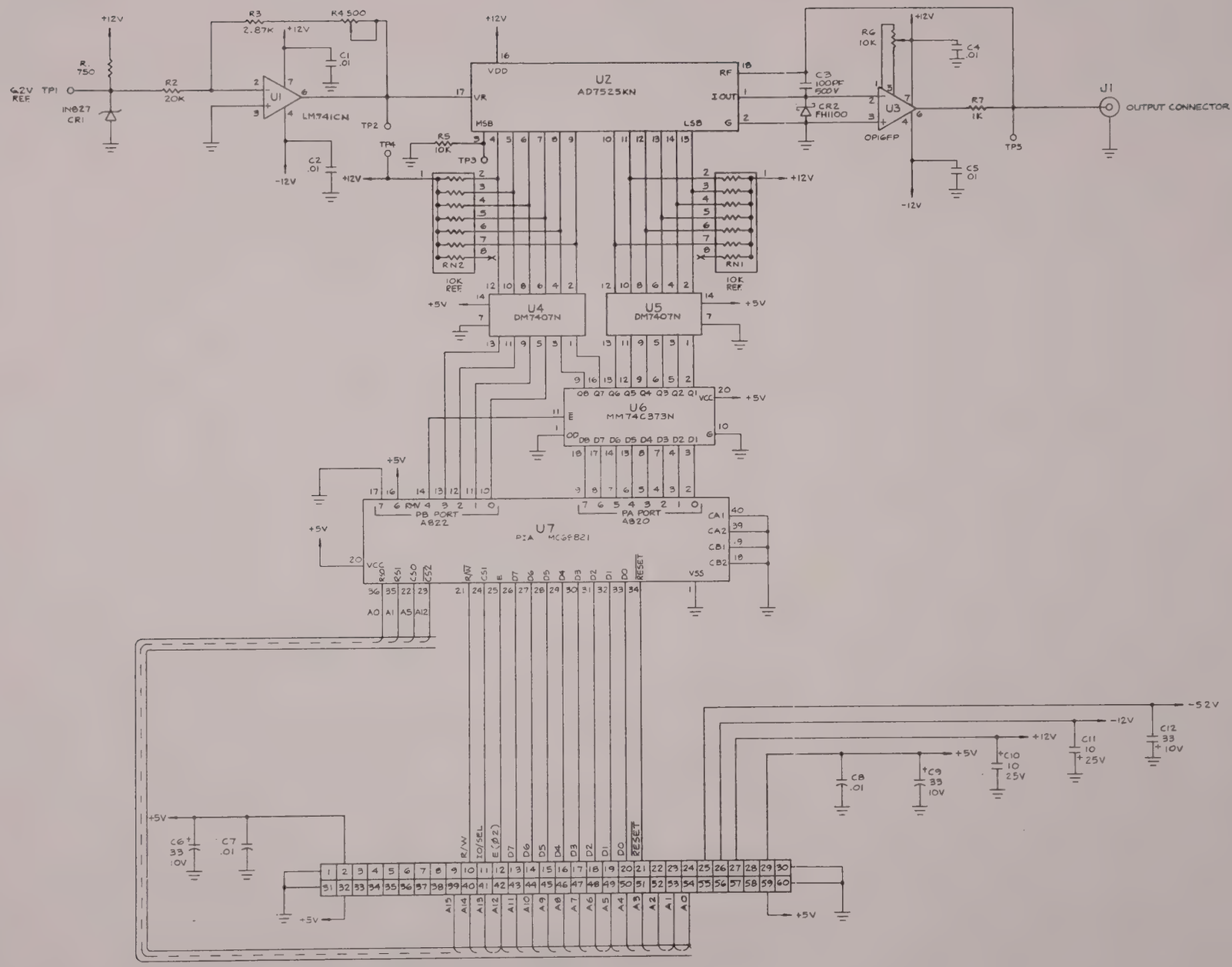


Figure 10–4. Component Locator, DAC

2020145–03



IC TABLE — P/N '40 —						
IC NUMBER	TYPE					
U1	LM741CN	3	7	4		
U2	AD7525KN	2	8			
U3	OP-16FP	3	7	4		
U4 U5	DM7407N	7			14	
U6	MM74C373N	0			20	
U7	PIA MC6821				20	

5500145-03

Figure 10-5. Schematic Diagram, DAC

OPTION 02
POWER MEASUREMENT

Option 02 measures the power of signals applied to Band 3. The power is displayed (to 0.1 dB resolution) simultaneously with frequency (to 100 kHz max. resolution). For AM and FM averaging purposes, gate time is controllable in the power meter mode, through the resolution function. Power gate time mirrors frequency gate time. For example, in resolution 0 the frequency gate time is 1 second, and the power gate time is 1 second. In resolution 1 the frequency gate time is 100 msec., and the power gate time is 100 msec. Option 02 allows power offsets from -99.9 dB to 99.9 dB, with a 0.1 dB resolution and will not degrade the basic performance of the counter.

SPECIFICATIONS

ACCURACY	±1.2 dB Typical 0-50° C ±0.5 dB Typical 25° C
TIME ADDED	1 GATE TIME + 50 msec.
RESOLUTION	0.1 dB POWER Sensitivity to -10 dBm; 0.2 dBm to OVERLOAD Selectable 100 kHz -1 GHz frequency.
RANGE	Entire Operating Range of Band 3

KEYBOARD OPERATION

To turn the power meter ON or OFF, press: POWER METER ON/OFF

If the power meter option is off, pushing the POWER METER ON/OFF key will turn the power meter on. Pushing that key again will turn the power meter off. If the counter is displaying only frequency it will begin displaying frequency and power. If the counter is displaying frequency and power it will begin displaying frequency only.

Turn the power meter on. Observe the display. Frequency is displayed on the left, and power is displayed on the right. The dBm annunciator lights to indicate power meter operation. If the power of the signal is too small to measure, the display will show EE.E in the power meter digits. (Since 0 dBm is a valid power 00.0 cannot be used as a no-power indicator.)

When the power meter option is on, the frequency measurements displayed on the front panel are to a maximum resolution of 100 kHz. The last selected time will be retained.

Power meter offset function enables the entry of a positive or negative power offset to 0.1 dB resolution. The offset will be incorporated into the power measurement after the next gate.

TO INPUT POWER OFFSETS

PRESS:	POWER METER OFFSET	Notice flashing annunciator and power offset last entered.
PRESS:	#	Number keys corresponding to desired power offset.

PRESS: dB To terminate input sequence. Notice OFFSET PWR annunciator solidly lit after terminator key is released.

TO RECALL STORED OFFSETS

PRESS: POWER METER OFFSET Stored offset is displayed.

PRESS: CLEAR DISPLAY Returns counter to display measurements.

TO REMOVE POWER OFFSETS

PRESS: POWER METER OFFSET DATA CLEAR OR POWER METER OFFSET 0 dB OR POWER METER OFFSET dB

GPIB OPERATION

PA – Power Active. Turns POWER METER option on.

PP – Power Passive. Turns POWER METER option off

PO – Power Offset. Enables entry of positive or negative power offsets to 0.1 dB resolution. Take a new reading after data entry if counter is not in HOLD.

THEORY OF OPERATION

The power meter uses the Schottky diode in the microwave converter as its power sensor. The output of the diode detector is connected to a programmable gain attenuator, which consists of two switchable gain stages (one is in the IF Amplifier A201B and one is on the Gate Generator A107) and two 8 bit attenuators. A comparator, set to 100 mV, and a TTL latch provide output information to the microprocessor. See Figure 11-7.

After the counter has a signal, and has taken a frequency reading, it starts the power meter task. This triggers the gate time counter, resets the TTL power latch, moves the YIG ±50 MHz (to insure that the signal peak is passed through), then checks the TTL power latch. If the latch is set, the attenuation is increased in 3 dB steps (until the signal is attenuated below the level of the comparitor), then back one step. If maximum attenuation is reached, and the latch is still being set, the word OVERLOAD is displayed and the task is exited.

When the latch is first checked, if it is still reset, the attenuation is decreased in 3 dB steps until the comparator level is reached. If minimum attenuation (maximum gain) is reached, the display is set to EE.E and the task is exited.

After the attenuation is adjusted to a 3 dB resolution, a successive approximation is performed to find the attenuation to a 0.1 dB resolution. The attenuation is stored, and if the gate time counter is not finished, the cycle is repeated. When the gate time counter is finished all the readings are averaged to eliminate the effects of AM on the signal.

The "power vs power" and "power vs frequency" corrections are added, and the sum is displayed. A detailed flowchart of the power meter is shown in Figure 11-8.

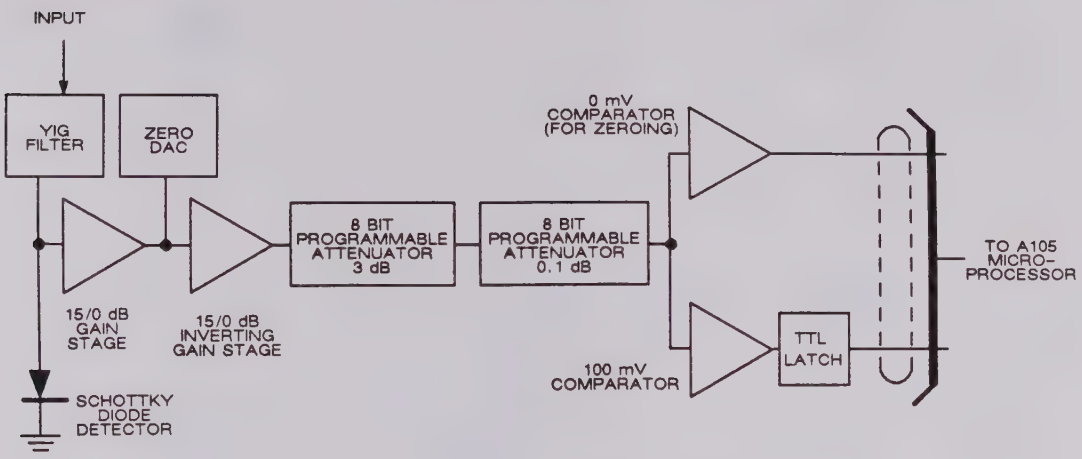


Figure 10-6. Power Meter Hardware

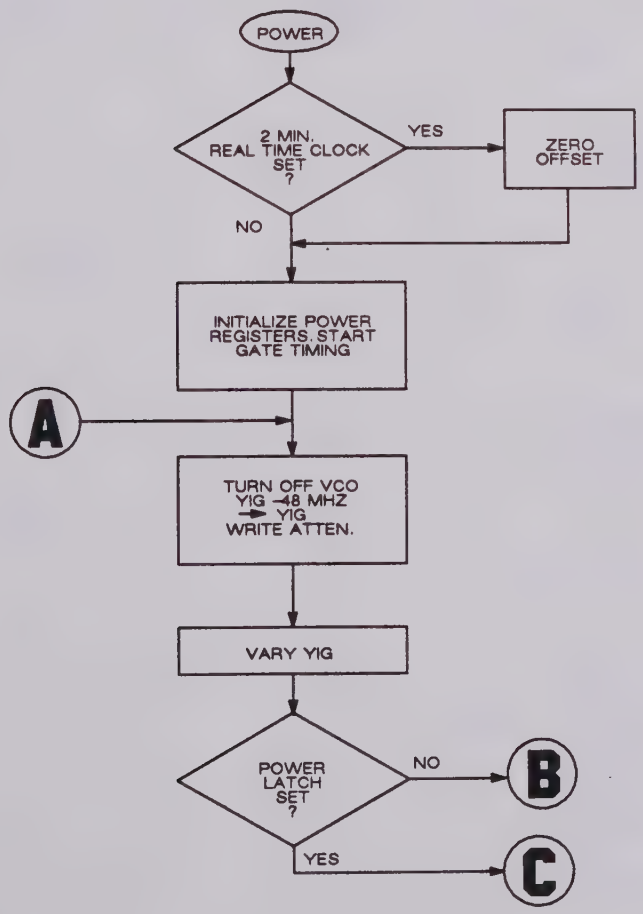


Figure 10-7. Power Meter Task

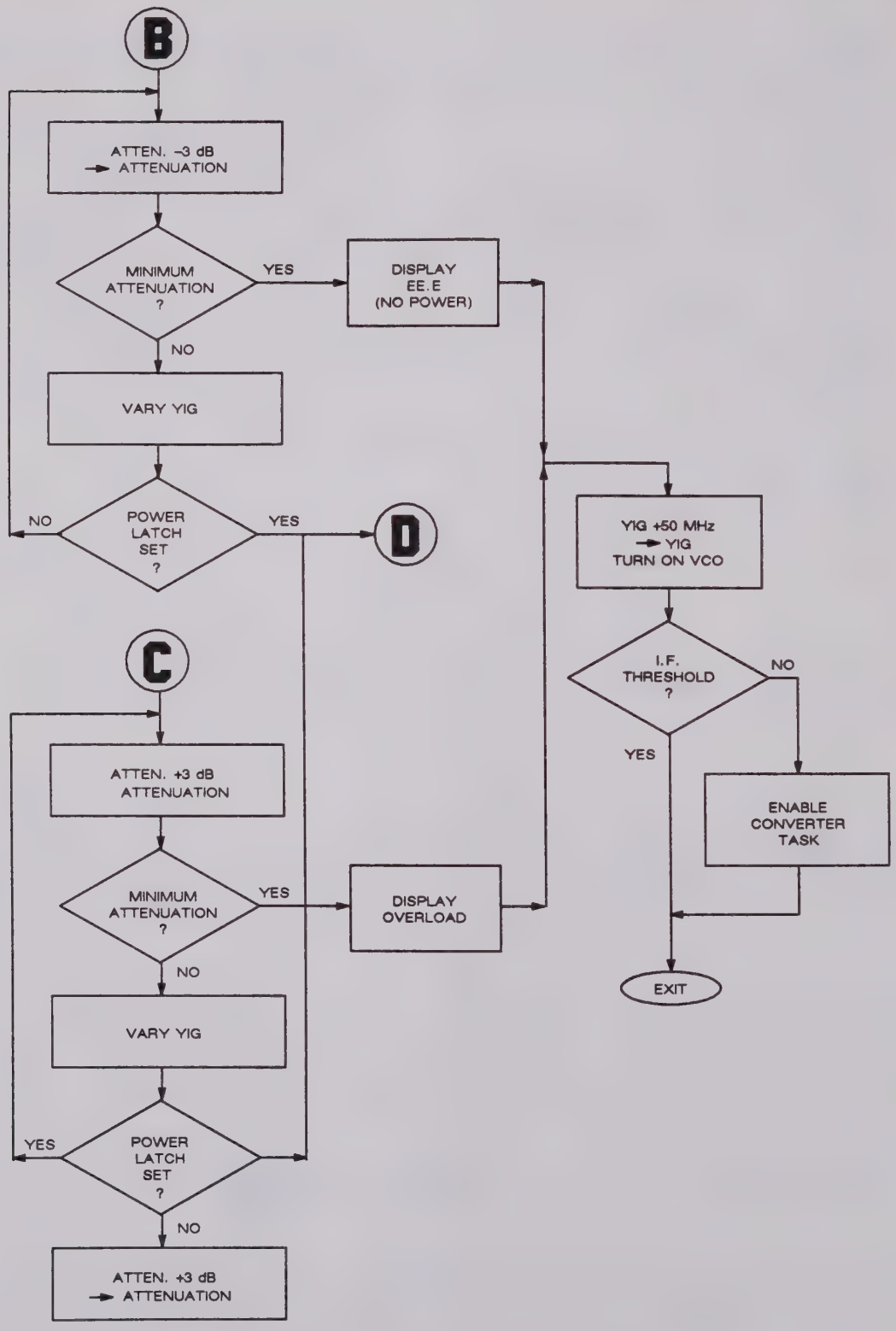


Figure 10-7. Power Meter Task, continued

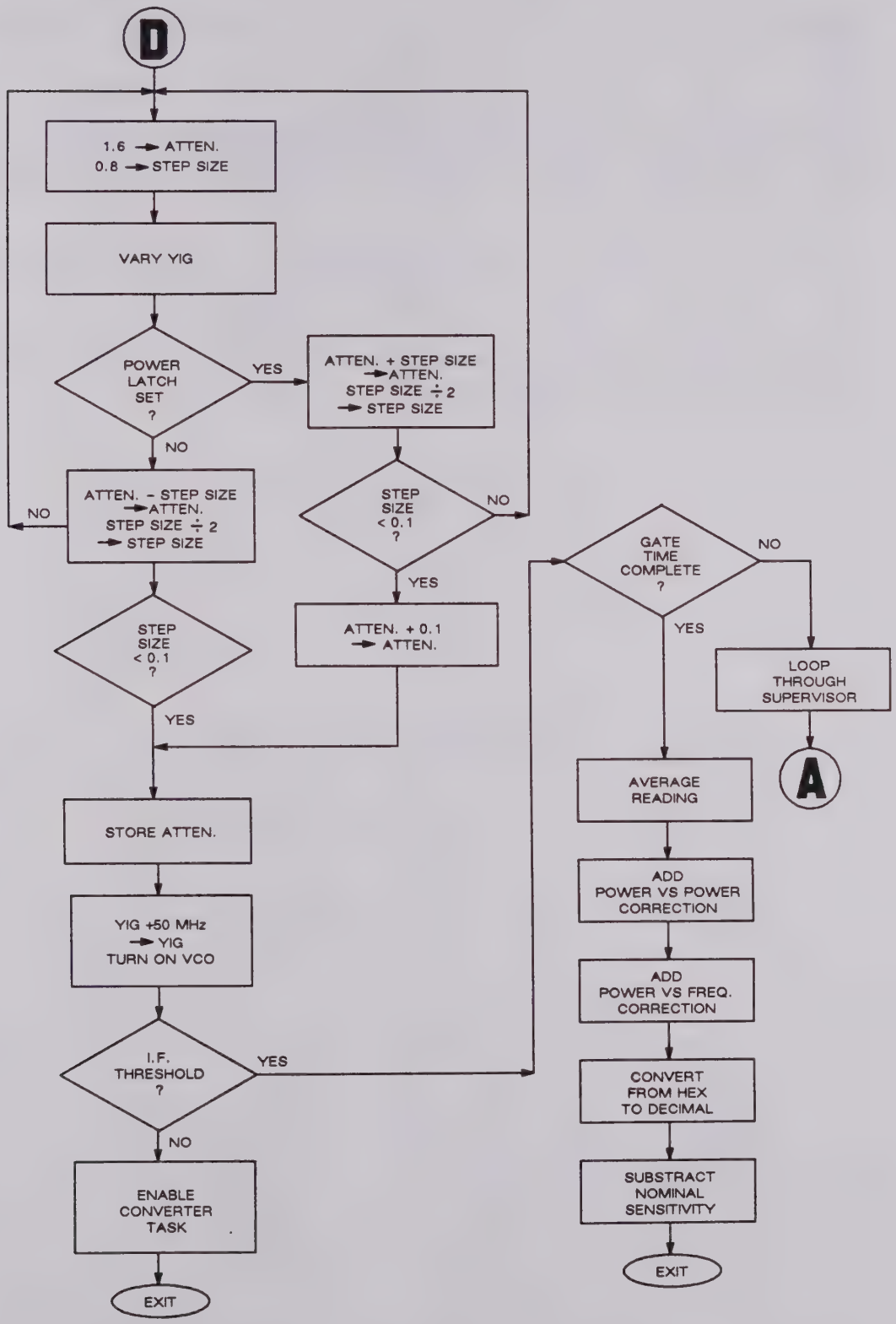


Figure 10-7. Power Meter Task, continued

CALIBRATION

The power meter contains 690 correction factors, stored in PROM.

The 150 "power vs power" correction factors compensate for variations from square law in the detector and power meter circuits. They are divided into three tables. The first table corrects variations below 10 GHz. The second corrects variations between 10 and 20 GHz. The third corrects variations above 20 GHz.

The 540 "power vs frequency" correction factors compensate for variations in the detector output at different frequencies. "Power vs frequency" corrections cover 0–27 GHz every 50 MHz.

The power meter is calibrated at the factory using specialized automatic test equipment. Recalibration in the field is not recommended.

OPTION 02 – GATE GENERATOR W/POWER MEASUREMENT 2020197-11

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,CER	.01µF	20%	100V	2150003-00	15
C2	C1						
C3		CAP,TANTALUM	33µF		10V	2300015-00	4
C4	C1						
C5	C1						
C6	C1						
C7	C1						
C8		CAP,MICA SEE NOTE 1	15PF	5%	500V	2260014-00	1
C9		CAP,TANTALUM	1µF		35V	2300008-00	1
C10		CAP,MICA	33PF	5%	500V	2260021-00	2
C11		CAP,MICA	100PF	5%	500V	2260034-00	1
C12	C10						
C13	C1						
C14	C1						
C15	C1						
C16		CAP,TANTALUM	10µF	20%	25V	2300029-00	2
C17	C1						
C18	C3						
C19	C3						
C20	C1						
C21	C1						
C22	C3						
C23	C1						
C24	C1						
C25	C16						
C26	C1						
CR1		DIODE,5082-2835,PSVT SCHOTTKY				2710004-00	2
CR2		DIODE,5082-2800,PSVT SCHOTTKY BARR				2710006-00	1
CR3	CR1						
CR4		DIODE,1N827,ZENER,6.2V				2700827-00	1
J1		CONN,PCB,RT ANGLE,3 PIN				2620132-00	2
J2		NOT USED					
J3	J1						
Q1		XSTR,2N4124,NPN,GP				4704124-00	4
Q2		XSTR,2N4126,PNP,GP				4704126-00	3
Q3	Q1						
Q4	Q2						
Q5	Q1						
Q6	Q2						
Q7	Q1						
Q8		XSTR,SD215,FET SW,N-CH,D-MOS				4710031-00	1
R1		RES,CC	10	1/4W	5%	4010100-00	2
R2		RES,CC	1K	1/4W	5%	4010102-00	2
R3		RES,CC	620	1/4W	5%	4010621-00	2
R4		RES,CC	2.2K	1/4W	5%	4010222-00	3
R5		RES,CC	220	1/4W	5%	4010221-00	2
R6		RES,CC	510	1/4W	5%	4010511-00	2
R7		RES,CC	200	1/4W	5%	4010201-00	1
R8		RES,CC	27	1/4W	5%	4010270-00	1
R9		RES,CC	300	1/4W	5%	4010301-00	1
R10		RES,CC	4.7K	1/4W	5%	4010472-00	6
R11	R1						
R12		RES,CC	2K	1/4W	5%	4010202-00	2
R13	R10						

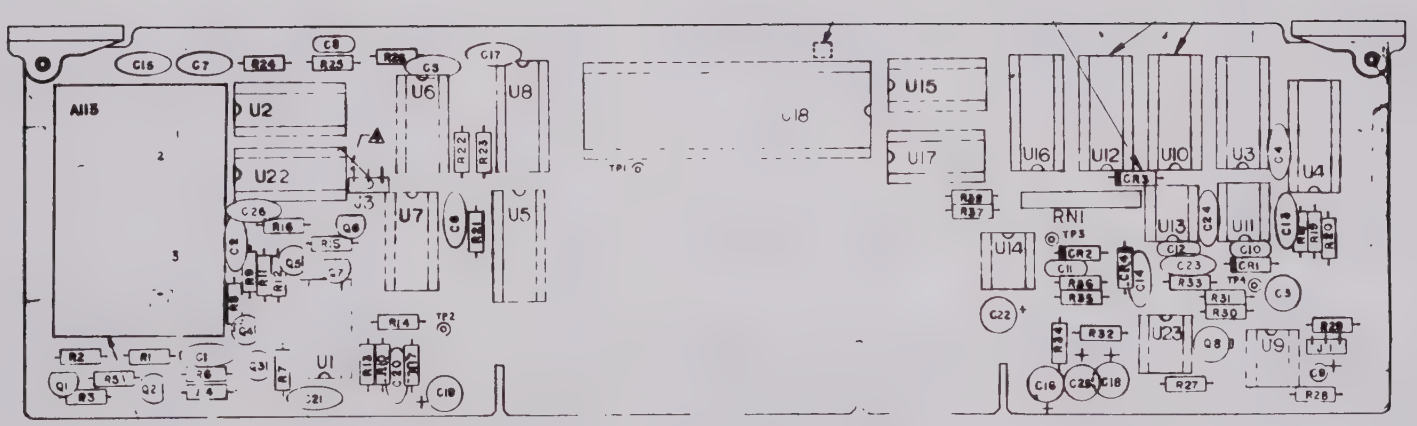
NOTE 1 – SAT AS FOLLOWS: 10PF MIN-36PF MAX

OPTION 02 – GATE GENERATOR W/POWER MEASUREMENT 2020197-11 (Continued)

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
R14	R4						
R15	R5						
R16	R6						
R17	R3						
R18		RES,M/OX	5.6K	1/4W	2%	4130562-00	1
R19		RES,M/OX	3.3K	1/4W	2%	4130332-00	1
R20		RES,M/OX	27	1/4W	2%	4130270-00	1
R21		RES,CC	2.7K	1/4W	5%	4010272-00	1
R22	R10						
R23	R10						
R24	R2						
R25	R12						
R26	R4						
R27		RES,M/OX	30K	1/4W	2%	4130303-00	1
R28		RES,M/OX	39K	1/4W	2%	4130393-00	1
R29		RES,MF	1.69K	1/10W	1%	4051691-00	1
R30		RES,MF	1.82K	1/10W	1%	4051821-00	1
R31		RES,MF	57.6K	1/10W	1%	4055762-00	1
R32		RES,CC	36K	1/4W	5%	4010363-00	1
R33		RES,CC	15K	1/4W	5%	4010153-00	1
R34		RES,M/OX	750	1/4W	2%	4130751-00	1
R35		RES,MF	6.19K	1/10W	1%	4056191-00	1
R36		RES,MF	100	1/8W	1%	4051000-00	1
R37	R10						
R38	R10						
RN1		RES,NTWK	5X10K	0.3W	2%	4170005-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	4
TP2	TP1						
TP3	TP1						
TP4	TP1						
U1		IC,74LS132				3084132-00	1
U2		IC,74LS490				3084490-00	1
U3		IC,AD7524J,DAC,8-BIT,1/2 LSB				3057524-00	2
U4	U3						
U5		IC,5009,P-CHANNEL MOS DIVIDER				3035009-00	1
U6		IC,74LS74				3087474-00	2
U7		IC,74LS02				3087402-00	1
U8		IC,10131,ECL 10K,M-S FF				3110131-00	1
U9		IC,5534,OPNL AMP,LOW NOISE				3045534-00	1
U10		IC,AD7524J,DAC,8-BIT,1/8 LSB				3057525-00	2
U11		IC,LM308A,OPNL AMP/BUFFER				3040308-00	2
U12	U10						
U13	U11						
U14		IC,LM393,VOLT COMP,LOW PWR				3050393-00	1
U15		IC,7407				3007407-00	1
U16		IC,4015,4-BIT STATIC SHIFT RGTR				3034015-00	1
U17	U6						
U18		IC,68B21P,PRPHL INTERFACE ADAPTER				3086821-00	1
U19		NOT USED					
U20		NOT USED					
U21		NOT USED					
U22		IC,74LS175				3084175-00	1
U23		IC,LM741C,OP AMP				3040741-00	1
XU1		CONN,SOCKET,DIP,14 PIN				2630015-00	5
XU2		CONN,SOCKET,DIP,16 PIN				2630016-00	9
XU3	XU2						

OPTION 02 – GATE GENERATOR W/POWER MEASUREMENT (Continued) 2020197-11

REF DES.	SAME AS	DESCRIPTION	EIP NO.	UNITS PER ASSY
XU4	XU2			
XU5	XU2			
XU6	XU1			
XU7	XU1			
XU8	XU2			
XU9		CONN,SOCKET,DIP,8 PIN	2630014-00	5
XU10	XU2			
XU11	XU9			
XU12	XU2			
XU13	XU9			
XU14	XU9			
XU15	XU1			
XU16	XU2			
XU17	XU1			
XU18		CONN,SOCKET,DIP,40 PIN	2630022-00	1
XU19		NOT USED		
XU20		NOT USED		
XU21		NOT USED		
XU22	XU2			
XU23	XU9			



2020197-11

Figure 10-8. Component Locator, Gate Generator

POWER METER ZERO DAC

REF OSC SELECTOR/DIVIDER

POWER METER

GATE GENERATOR

100 KHZ CLOCK

OPTIONS 05, 06, 07, 08 ONLY

HIGHEST REF. DE...							
C26	CR4	R38	28	L3	KN1	J3	
REF. DES. NOT USED							

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10,12 AD7524JN,LR	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC1013L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U22 SN74LS175	8	16			
U23 LM741CN				7	4

2. ALL .01 CAPACITORS ARE 100V.
   ALL CAPACITOR VALUES ARE IN MICRO-FARADS;
1. ALL RESISTORS ARE ±5%, 1/4 W.
   ALL RESISTOR VALUES ARE IN OHMS;

NOTES: UNLESS OTHERWISE SPECIFIED.

5500197-11

Figure 10-9. Schematic Diagram, Gate Generator

OPTIONS 03, 04, 05
TIME BASE OSCILLATORS

Three Time Base Oscillators are available as options for either the model 545B or 548B. These high stability options enhance the accuracy of the counter by the addition of oven stabilized crystal oscillators. These oscillators improve counter operation by reducing both time and temperature variations.

When any one of these options is installed, the TCXO is removed from the Gate Generator board (A107) and the following components are added.

- One of three Oven Oscillators (A114) mounted on the chassis.
- 28 VDC Power Supply board (A112), assembly part number 2010226-01.
- Power Supply Transformer T1 (part number 4900006-00) mounted on A112.
- Time Base Adjustment Pot J2 (part number 2010190-01) mounted on the rear panel.
- Related interconnecting cable harnesses.

	OPTION 03	OPTION 04	OPTION 05
CHARACTERISTIC	2030010-01	2030010-02	2030010-03
AGING RATE/24 HOURS (After 72 hour warm-up)	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-9} \rvert$	$< \lvert 5 \times 10^{-10} \rvert$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to + 50° C TEMPERATURE STABILITY	$< \lvert 6 \times 10^{-9} \rvert$	$< \lvert 3 \times 10^{-9} \rvert$	$< \lvert 3 \times 10^{-9} \rvert$
± 10% LINE VOLTAGE CHANGE	$< \lvert 5 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$	$< \lvert 2 \times 10^{-10} \rvert$

Figure 10-10. Time Base Oscillator Option Specifications

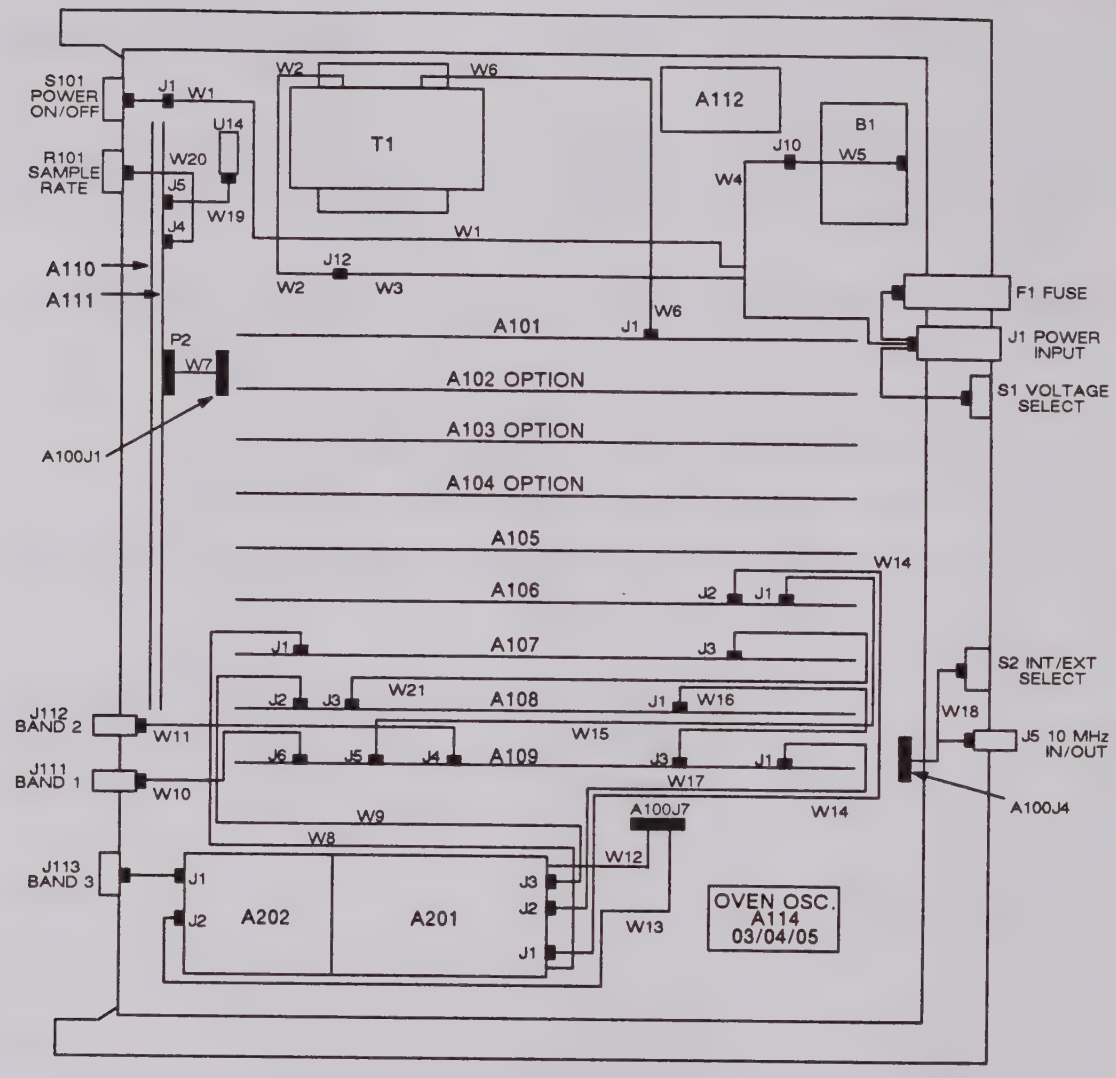


Figure 10-11. Component Location, Time Base Option

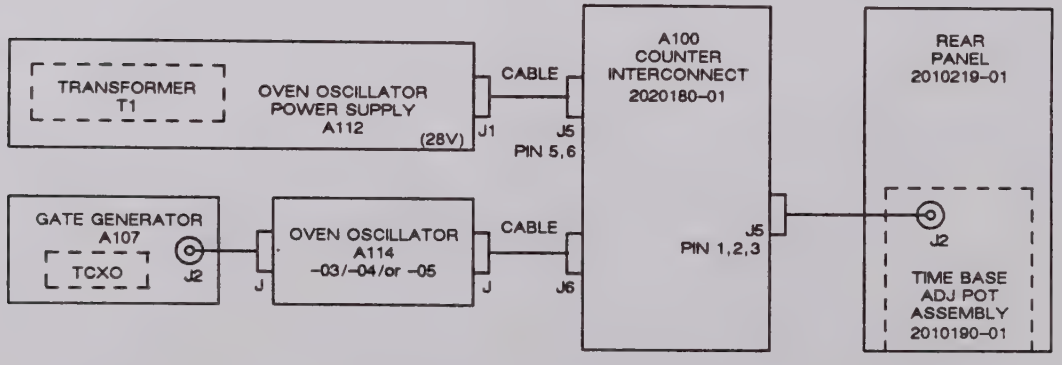


Figure 10-12. Interconnection Diagram, Time Base Option

OVEN OSCILLATOR POWER SUPPLY

The Oven Oscillator Power Supply board (A112) is a simple 28V regulated, current limited power supply. U1 and U2 provide voltage regulation, thermal protection and current limiting.

The transformer T1, CR1, C1 and C2 provide a 40V nominal unregulated DC voltage. The output voltage is set by voltage divider R5, R3 and R4. These resistors were selected so that 28V out provides 2.23V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground. See the schematic in Figure 10-15.

The power supply (A112) is on and operating as long as the counter is connected to an active AC power source. The counter's POWER ON/OFF switch on the front panel does not control this assembly.

OVEN OSCILLATOR CALIBRATION

When Options 03, 04 or 05 are installed in the counter, the effects of temperature perturbations and aging must still be considered, although the magnitude of the inaccuracies associated with each oscillator are greatly reduced.

Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of AC power). Under these conditions the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from +25° C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1 X 10^{-9} parts, relative to a standard, use this procedure. The test is illustrated in Figure 10-13.

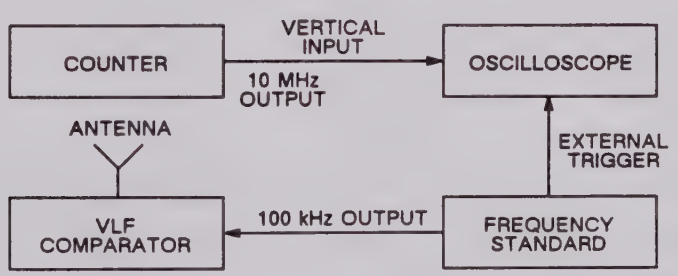


Figure 10-13. Time Base Calibration

All frequency checks and adjustments should be made only after the oscillator has been connected to its power source for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours it may require 72 hours of continuous operation to achieve the specified frequency aging rate.

To measure oscillator frequency:

1. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.

2. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.

3. Set oscilloscope sweep rate to 0.1 μ sec/cm.

4. Adjust oscilloscope vertical controls for maximum gain.

5. Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

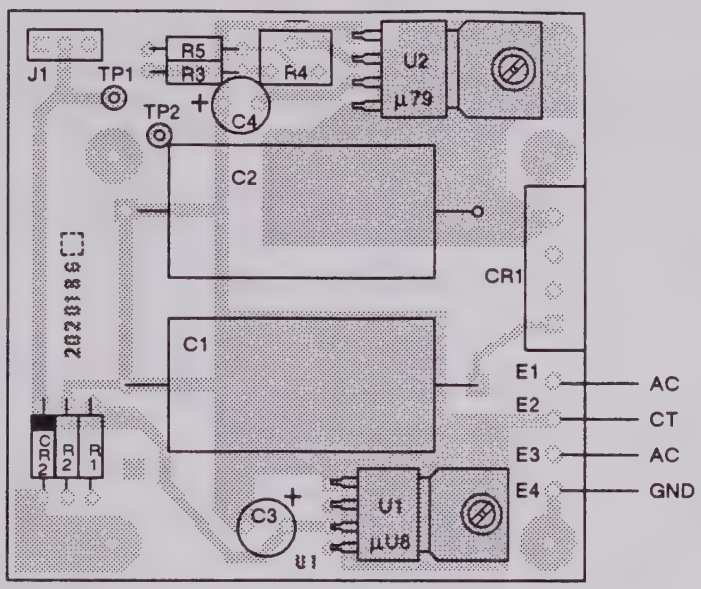
$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

   If the pattern drifts, at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.

6. Horizontal drift of oscilloscope display in μ sec/sec is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting.

NOTE

For higher accuracy, the counter should be operated for 72 hours prior to adjustment.



2020186-01

Figure 10-14. Oven Oscillator Power Supply (A112) Component Location

OPTIONS 03/04/05 - TIME BASE OSCILLATOR 2020186-01

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
C1		CAP,ELCTLT	680µF	10%	40V	2200021-00	2
C2	C1						
C3		CAP,TANTALUM	10µF	20%	25V	2300029-00	2
C4	C3						
CR1		DIODE,BR81D,BRIDGE,RECT				2710019-00	1
CR2		DIODE,1N4001,PWR RCT				2704001-00	1
J1		CONN,FRICT LK .100,3 PIN				2620121-00	1
R1		RES,M/OX	3.3K	1/4W	2%	4130332-00	1
R2		RES,M/OX	2K	1/4W	2%	4130202-00	1
R3		RES,M/OX	560	1/4W	2%	4130561-00	1
R4		POT,CERMET	500	705	0.5W	4250014-00	1
R5		RES,M/OX	3.6%	1/4W	2%	4130362-00	1
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	2
TP2	TP1						
U1		IC,UA78MG,VOLT RGLTR,POS,40V				3040780-00	1
U2		IC,UA79MG,VOLT RGLTR,NEG,40V				3040790-00	1

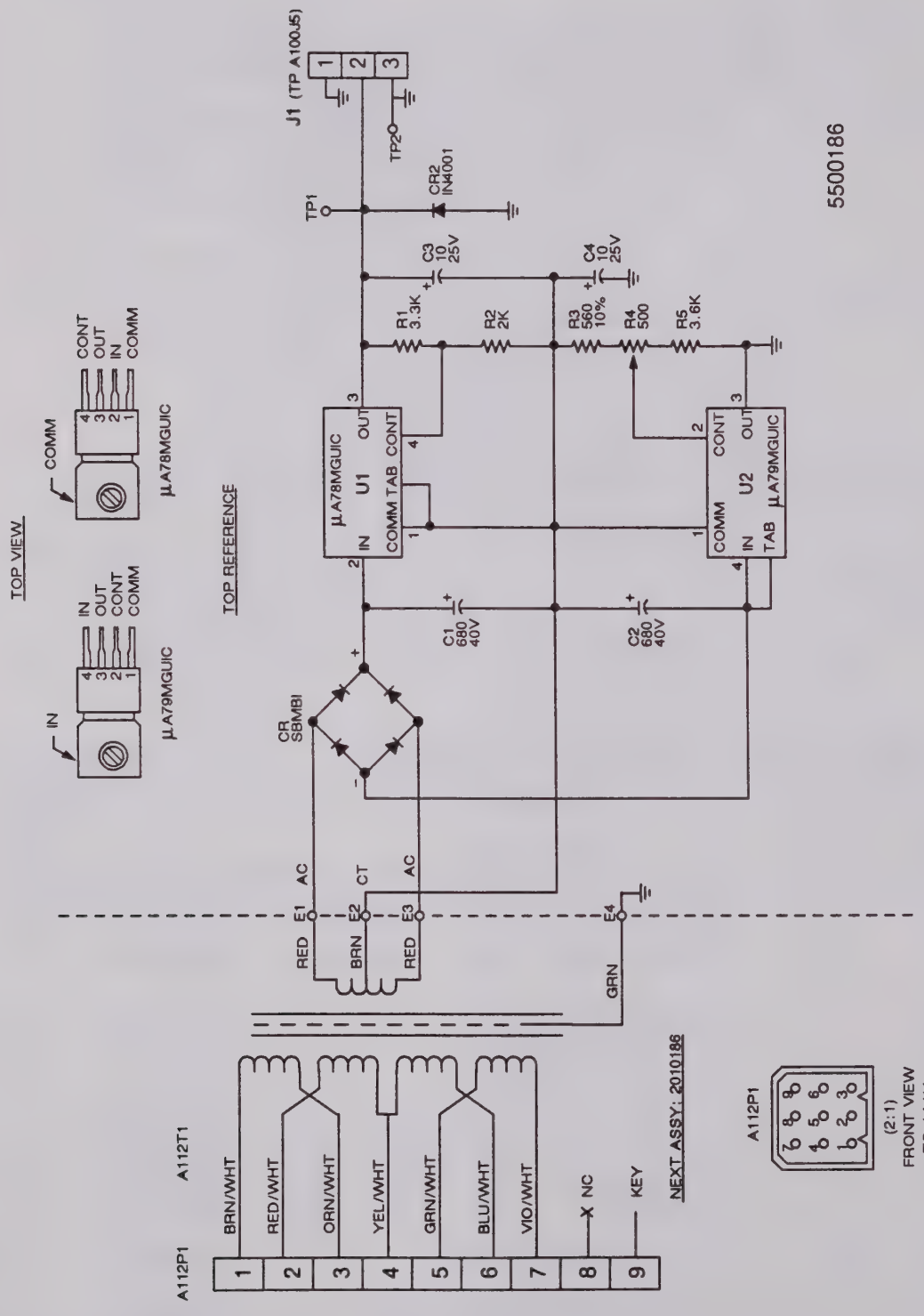


Figure 10-15. Time Base Option Schematic

OPTION 06
EXTENDED FREQUENCY CAPABILITY

The frequency range extension option is available on the 548B counter. This option, when used with the Model 590 Frequency Extension Cable Kit and one of the optional remote sensors, enables the counter to operate above 26.5 GHz. The option consists of:

- Band 4 Converter Module, A204
- Coax Cable, Front Panel to A204 J1 – P/N 2040232-01
- Coax Cable, Front Panel to A204 J2 – P/N 2040231-01

SPECIFICATIONS

BAND	FREQUENCY RANGE	SENSITIVITY (TYPICAL)	MAX. INPUT	REMOTE SENSOR MODEL
41	26.5 – 40 GHz	-25 dBm typ. -20 dBm min.	+5 dBm	91
42	40-60 GHz	-25 dBm	+5 dBm	92
43	60-90 GHz	-25 dBm	+5 dBm	93
44	90-110 GHz	-25 dBm	+5 dBm	94
42/43	50-75 GHz	-25 dBm	+5 dBm	95
41/42	33-50 GHz	-25 dBm	+5 dBm	96

KEYBOARD OPERATION

To operate the counter in one of the Band 4 frequency ranges, connect the short cable (supplied with the frequency extension kit) from the lower output jack on the front panel, to the Band 3 input. Connect the long cable from the upper jack to the remote sensor.

NOTE

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor. When you connect the sensor the counter will automatically display the reading.

To select Band 4:

PRESS: BAND — Band annunciator flashes

PRESS: 4 — Band 4 annunciator flashes

PRESS: # — Selected Band 4 annunciator lights stays on

The number should be between 1 and 4, corresponding to the desired frequency range. The counter is now in the proper mode for operation.

THEORY OF OPERATION - HARDWARE

When measuring a signal frequency greater than 26.5 GHz, the 578B using the Option 06 Frequency Extension with a Model 590 kit and a 91 remote sensor down converts the input to approximately 1.0 GHz. This signal is then fed to the Band 3 input, where a second conversion produces a 127 MHz IF.

A multiplier chain increases the VCO output frequency to the 5.28–6 GHz range, which is referenced to the time base. See Figure 10–16. This signal provides the local oscillator (LO) power, which is transmitted to the remote sensor, an external harmonic mixer. When the input frequency and harmonics of the LO, (generated in the mixer) combine, a first IF is generated in the range of 1.00–1.35 GHz.

A diplexer separates the LO and IF signals received from the harmonics mixer. The level of the IF is then increased to a minimum of –25 dBm via the IF amplifier, then supplied to the Band 3 converter input.

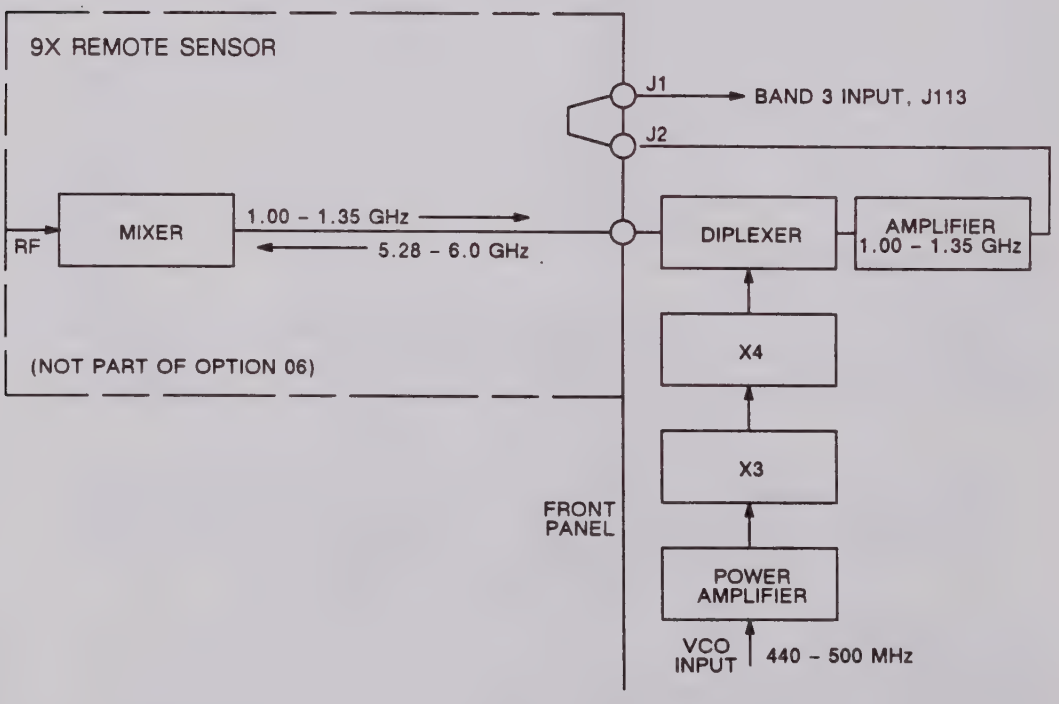


Figure 10–16. Frequency Extension Block Diagram

THEORY OF OPERATION - SOFTWARE (LOCKING ROUTINE)

The Band 4 software performs two main functions: it locks onto an incoming RF signal, and it tracks an RF signal once it is locked.

The locking routine is called by the supervisor when any of the following conditions are met:

1. Selection of Band 4
2. Software called from the source lock routine
3. Loss of IF threshold after being locked
4. Any reset condition

LOCKING PROCESS

INITIALIZATION

The initialization routine clears the working table (BANDTB) for Band 4 and loads from PROM the table of constants that is used by the program for the selected Band 4 subband. BANDTB is an area in RAM that is 40 bytes long.

VCO SWEEP

This routine steps the VCO frequency by a step size stored in BANDTB. After each step, it checks the VCO frequency for three stop points.

1. Top VCO frequency limit (depends on subband)
2. Wraparound frequency
3. Lockout frequency

If the top VCO frequency has been reached and no signal has been found, the program returns to the supervisor. If the top frequency is reached, and a signal has been detected, the VCO is set to its low limit and the bottom range is searched until the wraparound frequency is reached.

If the wraparound frequency has been reached (the frequency at which the last VCO frequency has produced the strongest IF signal), then the program stays at this frequency, and performs the centering and harmonic number calculation routines.

If a lockout frequency (a VCO frequency at which erroneous locking results) is detected, the VCO frequency will be incremented by :

8 * step size = new VCO frequency

and the program continues from this frequency.

After each VCO step, the YIG filter is swept to see if a signal is detected by the power DAC attenuator. If a signal is detected, the YIG is swept back and forth, and the attenuation is increased until the signal is lost. At this point a new VCO frequency is stepped and the process of signal detection continues and the power DAC is left at the last setting to detect the next highest signal.

CENTERING AND HARMONIC NUMBERING DETERMINATION

After the VCO sweep routine is complete and the VCO frequency is set, the incoming signal is mixed with a harmonic of the VCO frequency to produce a signal in a predetermined passband region (1.05 GHz to 1.25 GHz). Then a small VCO frequency is incremented to determine the mix side. After the VCO step, if the resulting IF increases, it is high side mix, otherwise, it is low side mix. The IF is then stepped to 1.05 GHz (or as close as possible) by using the following formula to calculate the VCO step size:

$$\frac{(\text{IF} - 1050\ \text{MHz}) * 100}{12 * \text{N\_MAX}}$$

Where N_MAX is the highest harmonic number allowed in the subband.

The above calculation is performed at most twice to bring the IF to 1.05 GHz. At this point the YIG is centered and the centering frequency FYIG1 and VCO frequency FVCO1 are stored. Next the VCO is stepped to bring the IF to around 1.25 GHz and a new centering takes place. This second center frequency is stored for later calculation of the harmonic number. Next the signal is stepped to its previous position and centered. This center frequency is now compared to FYIG1, and must be within 6 MHz. If it is not within 6 MHz, it is assumed that the signal is moving, and the Band 4 program exited.

The IF frequency step size, caused by the VCO frequency step, is used to determine the harmonic number by the following equation.

$$\frac{\Delta\ \text{IF FREQ. DUE TO VCO STEP}}{\text{HARMONIC SPACING}} = \text{HARMONIC \#(N)}$$

Where harmonic spacing = VCO step size X 12

CALCULATION ROUTINE – The calculation routine is used to find the approximate RF frequency F_{IN} in the following manner.

1. Compute F' = 12 N X F_{VCO}
2. Center the YIG filter on the first IF
3. Convert the binary YIG frequency to BCD
4. Compute F_{IN} = F' ± F_{YIG} (where F_{YIG} gives the approximate value for the first IF).
5. Compute a corrected VCO frequency using the equation:

$$F_{VCO} = (IF_{IN} \pm 127) / (12N \pm 2)$$

Then tune the VCO with the corrected frequency and center the first IF frequency in the YIG passband.

SHALLOW SEARCH – This routine tests for a signal in the IF passband. If a signal is present, the routine is exited. If a signal is not present, the routine will search an Rf range of ±60 MHz (in steps of 200 kHz), for the signal, and continues if a signal is found. If a signal is not found, the Band 4 program returns control to the supervisor.

BAND 4 TRACKING – The tracking routine centers the second IF in the following range.

115 MHz <2nd IF SIGNAL <135 MHz

This routine is called from outside of the Band 4 program to track a signal. A test is first made to determine if an IF threshold is present. If IF threshold is present it continues, if not the program returns to the supervisor to start the locking process from the beginning.

This routine reads the second IF frequency and computes the new VCO frequency so that the second IF is in the range given above. A new YIG frequency is calculated and the VCO and YIG are "tuned" to produce a new IF. A new FLO (frequency added to the second IF to produce the displayed frequency), is calculated. The equation for this process is:

$$F_{LO} = F_{VCO} (12\ N \pm 2)$$

The YIG frequency is: NEW F_{YIG} = 2 (NEW VCO) + 127 MHz.

PERFORMANCE TESTS

The Band 4 converter module is not field repairable. When a malfunction is suspected, its operation can be checked from the front panel as follows:

IF AMPLIFIER Apply a –50 dBm signal to the diplexer port (upper output jack) from 1.0 to 1.35 GHz. Output should be greater than –13 dBm as checked on a spectrum analyzer to the IF output (lower jack).

LO SIGNAL Connect a spectrum analyzer to the diplexer port (upper output jack). Using the following formula, set the VCO frequency between 440 and 500 MHz. The spectrum analyzer should show the 12th harmonic of the VCO frequency (5.28–6 GHz). The spectrum analyzer signal should be +8 dBm minimum, and free of breakup and spurious signals to –30 dBc.

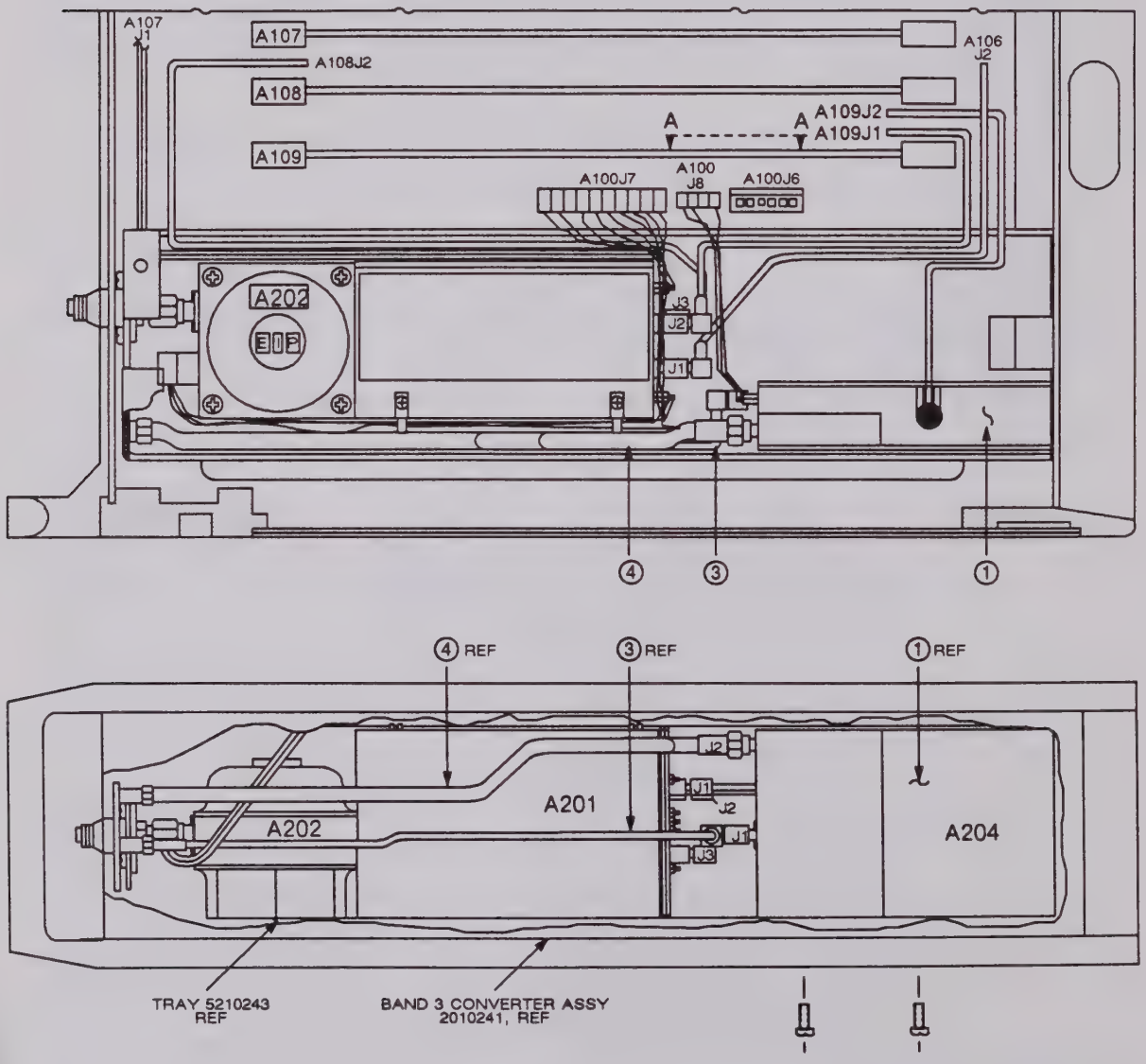
To convert from the desired VCO frequency to the PIA program number:

1. Round the desired frequency to a multiple of 50 kHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5 ... 440.75 X 5 = 2203.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 ..... 75 X 16 = 12
5. Add the result to the most significant digit from step 2 ..... MSD of 2203.75 = 2 – 2 + 12 = 14
6. Convert the result to hexadecimal ..... $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part ..... 2203.75 → E203
8. The two most significant digits are programmed to address 1822, and the two least significant digits are programmed to address 1820.

To remove a defective converter:

1. Remove the line cord and both the top and bottom cover of the counter.
2. Remove the two screws holding the converter in place from the bottom.
3. Remove coaxial cables and unplug DC harness.
4. Lift the converter out of the counter.

To replace, proceed in the reverse order. See Figure 10-17 for location of the converter in the counter.



① Band 4 Converter - 2010757

③ Cable (FP to A204J1) - 2040232-01

④ Cable (FP to A204J2) - 2040231-01

Figure 10-17. Location of Installed Band 4 Converter (A204)

OPTION 08
GENERAL PURPOSE INTERFACE BUS

The GPIB interface of the 545B/548B counters is fully compatible with the IEEE 488-1978 standard. With the GPIB interface, the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 Bus interface. At the simplest level, the counter can output data to devices such as a printer. In more sophisticated systems a calculator or other system controller can remotely program the counter, trigger measurements, and read results. Of course, a calculator or computer adds other benefits to a GPIB based measurement system. The calculator can manipulate data to compute the mean and standard deviation, check for linearity, compare results to limits, and perform many other functions.

GPIB FUNCTIONS IMPLEMENTED

The GPIB interface function subsets implemented are:

INTERFACE FUNCTION	SUBSET	DESCRIPTION
SOURCE HANDSHAKE	SH1	complete capability
ACCEPTOR HANDSHAKE	AH1	complete capability
TALKER	T5	basic talker, serial poll, Talk Only mode, unaddress if MLA
LISTENER	L3	basic listener, Listen Only mode, unaddress if MTA
SERVICE REQUEST	SR1	complete capability
REMOTE LOCAL	RL1	complete capability
DEVICE CLEAR	DC1	complete capability
DEVICE TRIGGER	DT1	complete capability

REMOTE LOCAL FUNCTION

When the counter changes from LOCAL to REMOTE or vice-versa, all the stored information is retained. The counter will operate in the same state as it was before the change. The only exception is when the counter is in the TEST mode, the TEST function is automatically terminated. When the counter is in REMOTE and LOCAL LOCKOUT is not active, the RESET key on the front panel keyboard acts as the return to local key.

DEVICE CLEAR FUNCTION

When the GPIB command DEVICE CLEAR or SELECTED DEVICE CLEAR is received, the counter will revert to its power on state as listed below:

Display Active
Band 3 Selected
Resolution 0
Fast Passive
Offset Active (Offset set to 0)
Power Meter Passive
Frequency Limit High set to default
Frequency Limit Low set to default
Test Passive (Clear Test Functions)
Exponent Zero (Output Format)
Service Request Passive

DEVICE TRIGGER FUNCTION

When the GPIB bus command DEVICE TRIGGER is received, the counter will initiate a new frequency reading cycle. The converter will not be reset. If the counter does not have a converter lock, the DEVICE TRIGGER will not be performed until a converter locked condition exists.

GPIB ADDRESS SELECTION

This counter employs a software selectable GPIB address which is stored in non-volatile memory. To verify the GPIB address, select Test 90: the counter will display the current GPIB address. Press the Clear Display key to exit Test 90 without changing the GPIB address.

To change the GPIB address, select Test 90 followed by the desired GPIB address (see Figure 10-18 for list of allowable GPIB address codes).

For example:

PRESS: TEST [9] [0] [2] [0] CLEAR DISPLAY Selects GPIB address 20

Since the GPIB address is stored in non-volatile memory, the counter will always default to the last GPIB address selected.

The GPIB address selection is also used to put the counter in the Talk Only (to) or Listen Only (lo) mode. To put the counter in the Listen Only mode simply set the address switch to any number 41 or higher.

TALK ONLY MODES

The TALK ONLY modes enable the counter to output data to other devices on the bus, such as a printer, without the need of an instrument controller. To use the counter in a TALK ONLY mode, enter the GPIB address corresponding to the desired mode of operation.

The counter can be put in four different modes of operation in the Talk Only mode. The following is a list of the address settings for entering these modes.

ADDRESS	MODE OF OPERATION
32	Continuous output determined by SAMPLE RATE control. Exponent in scientific format.
33	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in scientific format.
34	Continuous output determined by SAMPLE RATE control. Exponent in zero output format.
35	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in zero output format.

NOTE

In the Talk Only or the Listen Only mode, the address of the counter is always automatically set to decimal 0.

GPIB INSTRUCTION FORMAT

<OP CODE> <NUMBER> < TERMINATOR>

OPERATION CODE or OP CODE can take any of the following formats:

<LETTER> <LETTER> or <LETTER> <DIGIT>

Example: FH (Frequency Limit High) or B3 (Band 3)

The NUMBER portion of the statement can take the form of any of the following:

<SIGN> <DIGIT STRING>

Example: -2457

<SIGN> <DIGIT STRING> . <DIGIT STRING>

Example: -3.483

NOTE

Spaces within the <OP CODE> and <NUMBER> portions of the instructions are always ignored.

The TERMINATOR allows the operator to choose the scale of an input number as well as implement special functions.

TERMINATOR = G/M/K/H/D/P/C

G, M, K, H, represent GHz, MHz, kHz and Hz respectively

D = dB, P = clear data, (equivalent to "clear data" key on keyboard)

C = clear display (equivalent to "clear display" key on keyboard)

FORMAL DEFINITION OF INSTRUCTIONS

<OP CODE> <NUMBER> <TERMINATOR>

<OP CODE> ::= <LETTER> <LETTER> | <LETTER> <DIGIT>

<NUMBER> ::= <SIGN> <DIGIT STRING> |
<SING> <DIGIT STRING> . <DIGIT STRING> |
NULL

<TERMINATOR> ::= G | M | K | H | D | P | C | NULL

<SIGN> ::= + | - | NULL
<DIGIT STRING> :: = <DIGIT> <DIGIT> <DIGIT> .....

<LETTER> ::= A | B | C | D | E | F | G | H | I | J | K | L | M | N | O | P | Q | R | S |
T | U | V | W | X | Y | Z |

<DIGIT> ::= 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0

PROGRAM CODE SET

DISPLAY

DA – Display Active: Output Frequency Reading to Front Panel and Bus

DP – Display Passive: Output Frequency Reading to Bus only

DN – Display Normal

BAND

B1 – Band 1: 10 Hz – 100 MHz

B2 – Band 2: 10 MHz – 1 GHz

B3 – Band 3: 1 GHz – 20 GHz (Model 545B / 26.5 GHz (Model 548B)

B4 – Band 4: (Model 548B / Option 06)

RESOLUTION

R.1 – Resolution .1 = 0.1 Hz (Band 1 only)

R0 – Resolution 0 = 1 Hz

R1 – Resolution 1 = 10 Hz

R2 – Resolution 2 = 100 Hz

R3 – Resolution 3 = 1 KHz

R4 – Resolution 4 = 10 KHz

R5 – Resolution 5 = 100 KHz

R6 – Resolution 6 = 1 MHz

R7 – Resolution 7 = 10 MHz

R8 – Resolution 8 = 100 MHz

R9 – Resolution 9 = 1 GHz

MEASUREMENT FUNCTIONS

FA – Fast Active (Ignore sample rate Pot)

FP – Fast Passive (Terminates FA)

RS – Reset Basic Counter and Converter. Take a new reading after reset.

HA – Hold Active

HP – Hold Passive

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset. Take a new reading after data entry if counter not in hold.

PO – Power Offset. Take a new reading after data entry if counter not in hold.

OA* – Offset Active:

- Add Frequency Offset to Frequency Reading
- Add Power Offset to Power Reading if Power Meter Function is active

OP – Offset Passive (Terminates OA)

ML – Multiplier. Multiplies frequency readings by an integer number.

* In Start-up Condition, although OA is Active, "0" (zero) Frequency and Power Offsets are programmed.

POWER METER

PA – Power Meter Option Active. Initiate a new gate.

PP – Power Meter Option Passive (Terminates PA)

FREQUENCY LIMITS

FH – Frequency Limit High. Basic counter and converter will be reset after data entry.

FL – Frequency Limit Low. Basic counter and converter will be reset after data entry.

SELF-TEST FUNCTION

TA – Test Active.

TP – Test Passive. (clear test function)

DATA FORMAT

EZ – Exponent Zero

ES – Exponent Scientific

DATA OUTPUT

BR – Output both frequency and power readings

FR – Output frequency readings only

PR – Output power readings only

SERVICE REQUEST

SR – Service request enable

DAC OPTION

DC – Select DAC option

DESCRIPTION OF AVAILABLE COMMANDS

DISPLAY

DA – Display Active – Outputs readings to both front panel and GPIB bus.

DP – Display Passive – Outputs readings to GPIB bus only. It will decrease the cycle time of the counter.

DN – Display Normal – Resets display only; used for clearing error messages on the display. Cannot be used after verifying preprogrammed data such as Frequency Offsets or Frequency Limits. This OPCODE affects only the display.

BAND

B1 – Selects Band 1

B2 – Selects Band 2.

B3 – Selects Band 3.

B4 – Selects Band 4. See Option 06.

RESOLUTION

R.1 thru

R9 – Resolution .1 thru 9 – Picks the front panel resolution from .1 Hz to 1 GHz. Also chooses gate time which is related to resolution: .1 Hz = 10 sec, 1 Hz = 1 sec, 10 Hz = 100 msec, 100 Hz = 10 msec and 1 kHz to 1 GHz = 1 msec.

MEASUREMENT FUNCTIONS

FA – Fast Active – Causes the counter to go into the fast cycle mode of operation. In this mode, the front panel sample rate/hold control is inactive and the fastest sample rate is attained. The counter will not go into the Fast Active mode of operation until Hold Active is disabled.

FP – Fast Passive – Terminates FA.

RS – Reset Basic Counter and Converter – Reacquires input signal and takes a new reading. Has the same function as manual reset button.

HA – Hold Active – The counter stops taking readings and the last frequency and power readings are displayed and held. The counter can be directed to take one reading when it is in this mode by sending Device Trigger or Selected Device Trigger GPIB bus command to the counter. It will also update the reading if the RS mnemonic is received.

HP – Hold Passive – Terminates HA.

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset – Enables entry of frequency offsets. (1 Hz resolution available.) A new gate will be initiated after data entry if counter is not in HOLD.

PO – Power Offset – (See Option 02).

OA – Offset Active – Add frequency offset to frequency readings. Add power offset to power readings if power meter function is active.

OP – Offset Passive – Does not add frequency and power offset to readings.

ML – Multiplier – Enables entry of a 2-digit frequency readings multiplier. The multiplier must be an integer between 00 and 99. The results are to 1 kHz resolution. A new reading will be initiated after the data entry if the counter is not in HOLD. If the results of the multiplications are larger than or equal to 999.999,999,000 GHz, the counter will output 999.999,999,000 GHz to the bus if asked to output readings.

POWER METER

PA – Power Active (See Option 02).

PP – Power Passive (See Option 02).

FREQUENCY LIMITS

FH – Frequency Limit High – Enables entry of frequency limit high (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

FL – Frequency Limit Low – Enables entry of frequency limit low (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

SELF-TEST FUNCTIONS

TA – Test Active – Enables the counter to perform the selected test function by entering TA followed by two digits. When Test 05, 08, 09, or 10 is active and the counter is being asked to output data, the data that is displayed on the front panel is the data being output.

The output data format is as follows:

XXXXXXXXXXXXCRLF
X = alpha–numeric
CR = carriage return
LF = line feed

For detailed descriptions of tests 01 through 09 and test 11, see the section on Keyboard Controlled Circuit Tests.

TP – Test Passive – Terminates test function.

DATA FORMAT

EZ – Exponent Zero – output format.

ES – Exponent Scientific – output format.

DATA OUTPUT

BR – Output both frequency and power readings. (See section on output data format.)

FR – Output frequency readings only. (See section on output data format.)

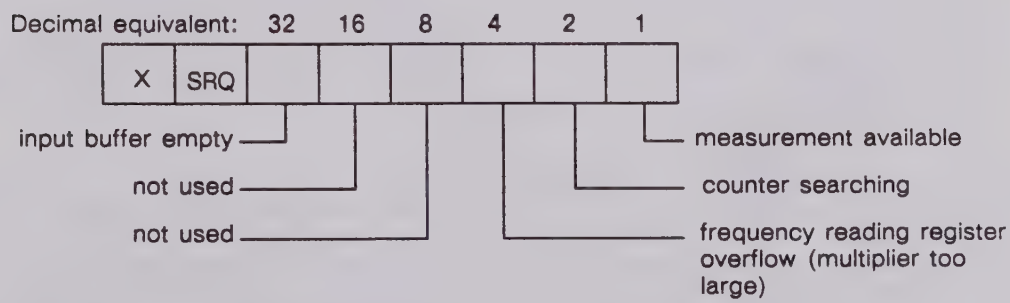
PR – Output power readings only. (See section on output data format.)

DAC OPTION

DC – DAC Option (See Option 01).

SERVICE REQUEST

SR – Service Request Enable – Enables the counter to send Service Request to the bus when a certain event has taken place in the counter. To enable the function, input SR followed by two decimal digits. The two digits are the decimal equivalent of the content of the eight bit status register. More than one bit of the status register can be set.



To disable the Service Request function, input SR00.

NOTE

Even when the Service Request function is disabled, the Service Request status byte will still be continuously altered to reflect the internal states of the counter.

SERVICE REQUEST MASK

The counter can be instructed to send an interrupt, by setting the SRQ line on the GPIB, when any ORed combination of the bits in the status byte are set. This is done by sending the counter a service request mask.

For example, to instruct the counter to generate an SRQ on measurement available OR input buffer empty, send the following service request mask:

```
OUTPUT 719;"SR33"
```

This would tell the counter to generate an SRQ whenever bit-0 or bit-5 of the status byte are set. Since bit-0 corresponds to measurement available and bit-5 corresponds to input buffer empty, the counter would generate an SRQ whenever either the input buffer was empty or a measurement was available.

The following items should be included in any program using the SRQ feature:

1. Tell the counter when to generate an SRQ. That is, tell the counter which events should generate an SRQ. This is done using the SRQMASK command.

2. Tell the controller to monitor the SRQ line on the GPIB. The SRQ is a maskable interrupt and the controller needs to know if it should respond to the interrupt.

3. Tell the controller what to do when it receives an SRQ interrupt.

4. Serial Poll the counter after an SRQ is generated to clear the interrupt. When the counter generates a SRQ it sets bit-6 in the status byte. Serial polling the instrument clears the SRQ bit and allows the instrument to generate a new SRQ upon the next occurrence of the conditions specified in the SRQ Mask.

5. It may also be necessary to clear the SRQ register in the controller. Consult your manual on the controller for more information on clearing the SRQ register in the controller.

The following program, written on a HP-9826, demonstrates how to use the SRQ feature to obtain a valid measurement from the counter.

```
10   ASSIGN @COUNTER TO 719          ! Assigns 719 to address variable
                                     ! The number 7 is the GPIB interface
                                     ! and 19 is the counters GPIB address
20   REMOTE @COUNTER;                ! Place counter in Remote
30   OUTPUT @COUNTER;"SR01"          ! Send SRQ mask to counter
40   ENABLE INTR 7;2                 ! Enable interrupt in controller
50   ON INTER 7 GOTO FLAG            ! Tell controller how to handle interrupt
70   WAITING:                        ! Label
60   PRINT "WAITING FOR VALID MEASUREMENT"
80   GOTO WAITING
90   FLAG: PRINT "***** SRQ RECEIVED *****"
100  ENTER @COUNTER;FREQ             ! Input Frequency from counter
110  PRINT "FREQ = ";FREQ            ! Print Frequency
120  S2 = SPOLL(@COUNTER)            ! Clear SRQ bit in counter
130  STATUS 7,4;S                    ! Clear SRQ bit in controller
140  OUTPUT @COUNTER;"SR00"          ! Turn off SRQ mask in counter
150  OFF INTR 7                      ! Turn off interrupt in controller
160  END                             ! Program end
```

To demonstrate this program, set up counter with no signal applied and start the program running. The controller should continually print out "Waiting for measurement." Then apply a signal. As soon as the counter finds the signal and counts it, the controller will print out the frequency of the signal.

DATA OUTPUT FORMAT

The 545B/548B transmit the following string of characters to output a measurement.

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Format																		
EZ (Exponent Zero)	b	±	D	D	D	D	D	D	D	D	D	D	D	D	E	0	CR	LF
ES (Exponent SCI)*	±	D	D	D	D	D	D	D	D	D	D	D	D	D	E	D	CR	LF
Power**	b	b	b	b	b	b	b	b	b	b	±	D	D	D	.	D	CR	LF

Freq. + Power

- FREQ in EZ mode: b ± D D D D D D D D D D D E 0, b b b b b b b b b b ± D D D . D CR LF
- FREQ in ES mode: ± D D D D D D D D D D D D E D, b b b b b b b b b b ± D D D . D CR LF

When the counter is in Test 05, 08, 09, or 10, the output will reflect the data on the display. The format is as follows:

XXXXXXXXXXXXCRLF.

b = Blank

D = Digit

X = Alpha-numeric

CR = Carriage Return

LF = Line Feed

* In Exponent Scientific one digit represents the position of the decimal point. Exponent digit can be either 0, 3, 6, or 9.

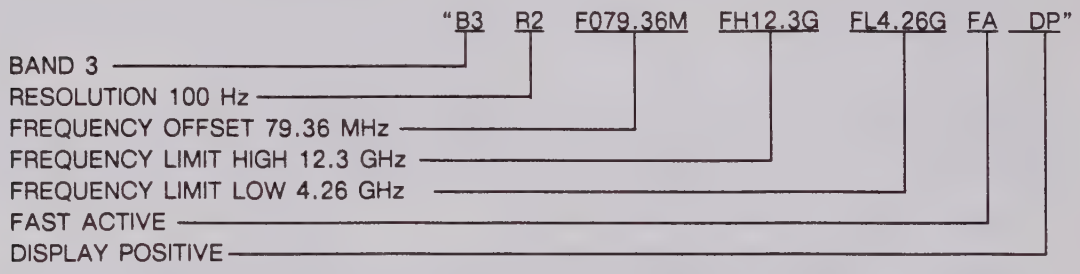
** The power information always have the decimal point fixed for 0.1 dB resolution.

Under different output modes, the following counter outputs can be expected by a listener.

OUTPUT MODE	COUNTER OPERATING MODE	OUTPUT
BR	PA	FREQ = PWR
	PP	FREQ
	TA01	FREQ
FR	PA	FREQ
	PP	FREQ
	TA01	FREQ
PR	PA	PWR
	PP	-999.9
	TA01	-999.9
BR, FR or PR	TA05, 08, 09, or 10	Data on front panel display

PROGRAM EXAMPLES

The examples given here assume an address setting of decimal 19 or ASCII talk address "S" and listen address "3" for the counter. By addressing the counter to listen and sending the following program string, it sets up the following measurement conditions.



The following programs illustrate how controllers function with the counter. These programs cause the counter to make a series of frequency measurements. The calculators read the measurements into memory and print the results. The programs assume the counter Talk and Listen address is decimal "19."

```
HP 9825A    0:   dim A (10)
            1:   rem 7
            2:   wrt 719, "B3R2FO-4.55M"
            3:   wait 300
            4:   for I = 1 to 10
            5:   red 719, A (I)
            6:   prt A (I)
            7:   next I
            8:   end
HP9845A     10:  OUTPUT 719, "B3R2FO - 4.55M"
            15:  WAIT 300
            20:  INPUT 719, A
            30:  PRINT "Frequency minus offset equals," A
            40:  GOTO 20
TEK 4051    10:  PRINT @ 19:  "B3R2FO - 4.55M"
            20:  INPUT @ 19: A
            30:  PRINT "Frequency minus offset equals," A
            40:  GOTO 20
```

The 9825A program will cause the counter to take a series of ten readings, print them on the 9825A paper tape and stop. Notice that an offset of 4.55 MHz is subtracted from each readings.

The program shown for the 9845A and TEK 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a "STOP" command. This is accomplished on the 9845A with the key labeled "STOP." On the TEK 4051 use the key labeled "BREAK." To restart the program enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

READING A MEASUREMENT

To read a measurement from the counter to a calculator, the counter must first be addressed to talk and the calculator to listen. The examples below indicate how a calculator may read a measurement from the counter.

HP 9825A

```
10 red 719, A
20 prt A
```

TEK 4051

```
10 INPUT @ 19:A
20 PRINT A
```

HP 9845A

```
10 ENTER 719, A
20 PRINT A
```

The EIP counters can use two different modes. HA which takes one reading then waits for a reset command or a Device Trigger GPIB Bus Command. In this condition the counter is sent a reset or Device Trigger and (when addressed to talk) a new reading is output to the BUS. The counter will hold that particular reading on the display until another reset command or Device Trigger command is received. The other mode is HP or HOLD PASSIVE. In this mode data is read out in a normal BUS fashion. The display automatically updates corresponding to the sample rate chosen. In this condition successive readings can be output without generating a reset or Device Trigger command each time.

INPUT SPEED

It takes a specific amount of time for the counter to process the input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus, and is temporarily stored in memory. The size of the storage memory is 100 characters.

The users of the GPIB interface need to be aware of the difference between accepting data and complying with it. If the counter is asked to output a reading before it has finished processing the input data, the output will be in error if the operator makes the assumption that the counter is in the mode that was just programmed. To prevent this, sufficient programmed delays must be provided, or use must be made of the counter's Service Request status byte. See Service Request (SR) command description.

**ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary					decimal
		5	4	3	2	1	*
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
"	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
‘	L	0	1	1	0	0	12
–	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

** Address characters in ASCII code.

Figure 10–18. Allowable Address Codes

OPTION 08 – GENERAL PURPOSE INTERFACE BUS 2020133-03

REF DES.	SAME AS	DESCRIPTION				EIP NO.	UNITS PER ASSY
		GPIB OPTION				2010635-01	
		CABLE ASSY,FLAT RBN,GPIB,OPT 08				2040177-01	
		PLATE,REAR PANEL,GPIB,54XA				5210297-00	
		GPIB BOARD				2020133-03	
C1		CAP,CER	.01µF	20%	100V	2150003-00	3
C2	C1						
C3	C1						
C4		CAP,TANTALUM	33µF		10V	2300015-00	2
C5	C4						
R1		NOT USED					
R2		NOT USED					
R3		NOT USED					
R4		NOT USED					
R5		NOT USED					
R6		NOT USED					
R7		NOT USED					
R8		NOT USED					
SW1A		NOT USED					
SW1B		NOT USED					
TP1		CONN,PCB,.040D PIN,GOLD				2620032-00	6
TP2	TP1						
TP3	TP1						
TP4	TP1						
TP5	TP1						
TP6	TP1						
U1		IC,3448A,XCVR,GPIB				3053448-00	4
U2	U1						
U3	U1						
U4	U1						
U5		IC,74LS04				3087404-00	1
U6		IC,68B488P,GP INTERFACE ADAPTER				3050027-00	1
U7		IC,74LS10				3087410-00	1
U8		NOT USED					
XU1		CONN,SOCKET,DIP,16 PIN				2630016-00	4
XU2	XU1						
XU3	XU1						
XU4	XU1						
XU5		CONN,SOCKET,DIP,14 PIN				2630015-00	2
XU6		CONN,SOCKET,DIP,40 PIN				2630022-00	1
XU7	XU5						

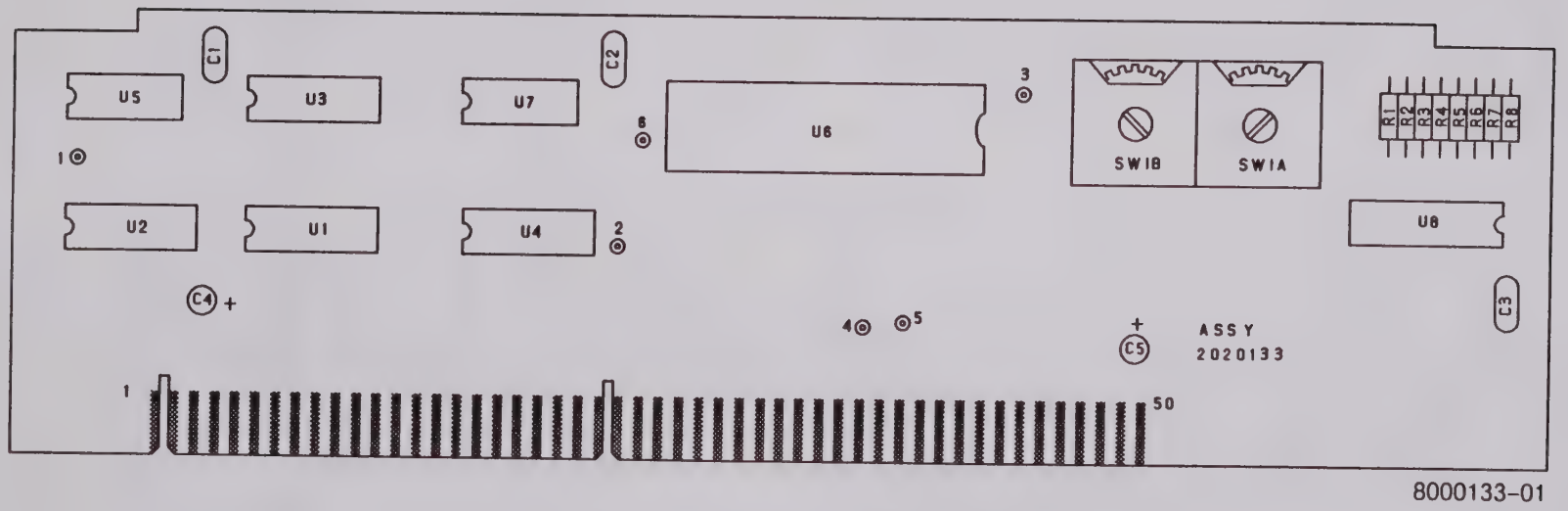
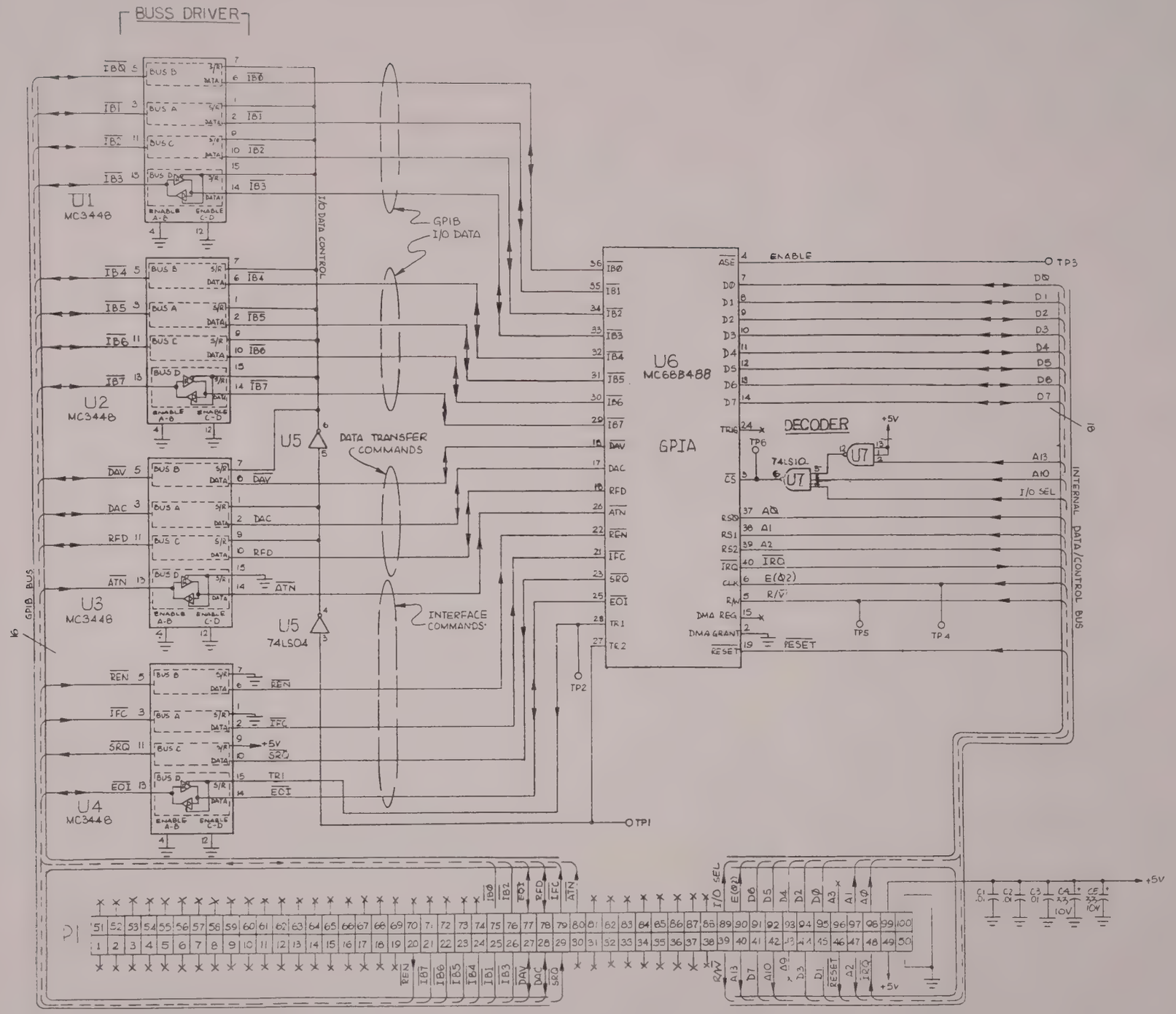
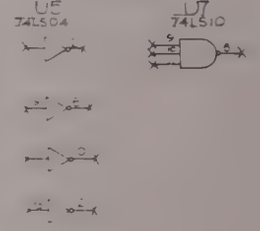


Figure 10-19. Component Locator, GPIB



IC NO.	TYPE	PIN NO.	
		GND	+5V
U1 U2, U3, U4	MC3448	8	16
U5	74LS04	7	14
U6	MC68488	1	20
U7	74LS10	7	14

NOT USED



5500133-03

Figure 10-20. Schematic Diagram, GPIB

OPTION 09
REAR PANEL INPUT

Option 09 provides rear panel input for 545B/548B counters, and counters equipped with Option 06 in the following manner:

545B/548B COUNTERS

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113.

2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

OPTION 06 EQUIPPED COUNTERS

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113. Reversing the Remote Sensor and Band 3 jumper connectors to the holes marked J114A (Rmt. Sensor) and J114B (Band 3 Connector) respectively.

2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

NOTE

The specifications for the counter do not change when the input is from the rear panel.

OPTION 10
CHASSIS SLIDE

Option 10 equips your counter with the hardware required to mount the unit in a standard 19" wide console. With the chassis slide installed the counter can be serviced without removing it from the rack.

The option consists of:

OPTION 10 - 2010147-02

①	Rack Mount Kit	- 2010008-01
②	Slide Set	- 5000365-00
③	Spacer, Slide	- 5210249-00
④	Chassis Slide Panel, Side	- 5210179-02

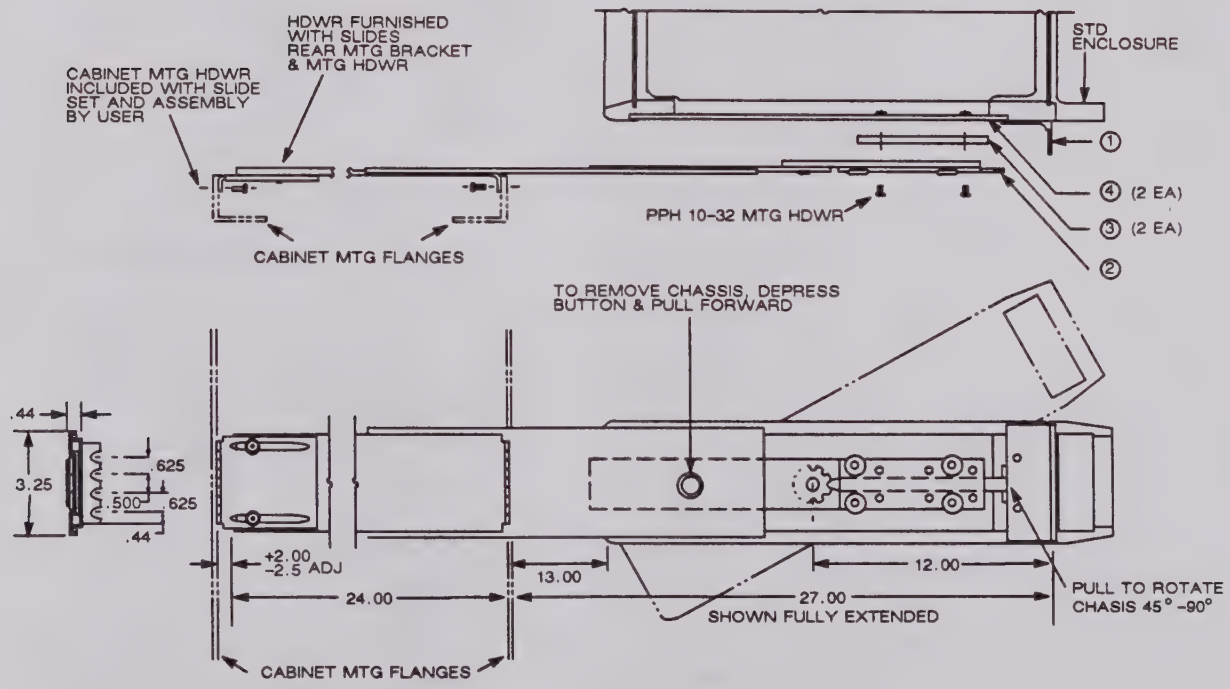


Figure 10-21. Chassis Slide

1. All MTG HDWR and hole spacing conforms to MIL-STD-189.
2. To install slides in field; Remove top cover and top frame; Mount special side panels (5210179-00) on Std. enclosure.
3. Item numbers within O symbol are P/L 2010147-02. All other items assembled or exploded are shown for clarification or reference only.

Side View of Counter With Option 10 Installed

Appendix A
Accessories

MODEL 590 FREQUENCY EXTENSION CABLE KIT

The kit, part number 2000025-02 contains:

1 - LO Cable (long) - 2040217
1 - IF Cable (short) - 2040218-01
1 - Adaptor (SMA to TNC) - 2610063-00
0 - 5 - Remote Sensors (Options 91 thru 96)

REMOTE SENSOR OPTIONS

	PART NUMBER	FREQUENCY RANGE
91	2030022-00	26.5 - 40 GHz
92	2030029-00	40 - 60 GHz
93	2030030-00	60 - 90 GHz
94	2030031-00	90 - 110 GHz
95	2030038-00	50 - 75 GHz
96	2030059-00	33 - 50 GHz

SPECIFICATIONS

Table A-1.

BAND 4 Used with 548B/06 Counter and 590 Frequency Extension Kit						
OPTION	91	92	93	94	95	96
SELECT BAND	41	42	43	44	42 or 43	41 or 42
Waveguide Band	Ka	U	E	W	V	Q
Range	26.5-40 GHz	40-60 GHz	60-90 GHz	90-110 GHz	50-75 GHz	33-50 GHz
Sensitivity (typ)	-25dBm (-20 dBm min.)	-25 dBm	-25 dBm	-25 dBm	-25 dBm	-25 dBm
Waveguide Size	WR-28	WR-19	WR-12	WR-10	WR-15	WR-22
Waveguide Flange	UG-599/U	UG-383/U	UG-387/U	UG-387/U	UG-385/U	UG-383/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm	+10 dBm
Aquisition Time	<1 sec	<1 sec	<1 sec	<1 sec	<1 sec	<1 sec

INSTALLATION

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor.

Connect the long LO cable from the upper jack to the remote sensor. When using the sensor option 91, use the SMA-TNC adapter in the 590 kit.

Connect the short IF cable from the lower jack to the Band 3 input.

CAUTION

Static discharge or ground loops can damage or destroy the diode in a remote sensor. ALWAYS connect the LO cable to the counter first, then touch the shield to the body of the sensor before connecting.

Be sure that the counter and waveguide port to which the sensor will connect have a common ground. If in doubt, connect with a ground strap before connecting the remote sensor.

OPERATION

After connection, select band 41,42,43, or 44 on the 578B counter (equipped with option 06). Select the band by:

PRESS: [BAND] [4] [1] or 42, 43, or 44.

Be certain that the band selected coincides with the remote sensor in use. See specifications in Table A-1.

NOTE

Frequency limits (low/high) and power meter function (Option 02) only operate to 26.5 GHz.

REPAIR

If loss of sensitivity occurs, the diode may be damaged. The 91 sensor diode can be replaced. All others require factory repair.

To replace the 91 sensor diode, unscrew the knurled cap and pull out the diode. Replace it with a 1N53B type diode that can be ordered from the manufacturer:

Alpha Industries, Inc.
20 Sylvan Road
Woburn MA 0-807

Or order from EIP by part number 2730053-00.

EIP has an assembly exchange program for rapid repair of damaged units. Consult factory for details.

SERVICE KIT

The service kit for the 545B/548B counter contains the following items and the kit itself is useful as a carrying case.

2000017-01	Service Kit
2020147-01	GPIB/BCD Extender Board
2020184-01	Standard Extender Board
2020185-01	Band 2 Extender Board
2040221-01	Cable, BNC to Select
2040222-01	Cable, BNC to PC JK
2610054-00	Test Cable, BNC E/Z Hook
5000094-00	IC Extractor Tool

This kit comes in a useful carrying case.

MP MASTER
MA28823